GEFÖRDERT VOM

Bundesministeri für Bildung und Forschung

On the Architecture of System Verification Environments

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Haifa Verification Conference, 2007

- Funded by the German government
- Partners from industry and academia
- Goal: pervasively verify four computer systems, three of which in industrial context
 improve quality, increase productivity

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Outline

- Verisoft Systems and System Layers
- Verified Stacks
 - Computational Models Stack
 - Semantics Stack
 - Example
- Verisoft Repository and Publication
- Conclusion



Scenario: general-purpose computer system

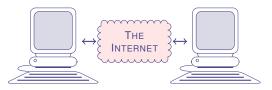
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- Scenario: general-purpose computer system
- Hardware, microkernel, operating system, applications



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- Services: user processes may use file I/O, IPC, networking via sockets, and RPC
- Application example: everything required to write, sign, send, and receive email

SP4 Verisoft Biometric Identification System



 Scenario: biometric sensor used to authenticate user against biometric reference data stored on smartcard

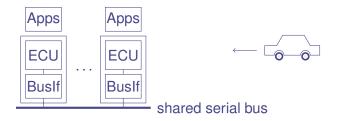
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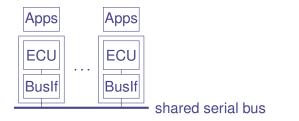
- Scenario: biometric sensor used to authenticate user against biometric reference data stored on smartcard
- Biometric data must be protected (according to German privacy regulations)
- Cryptographic protocol between smartcard and system



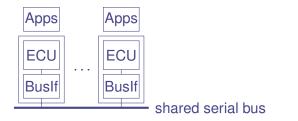
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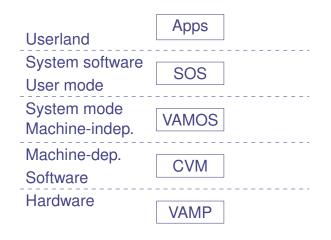
 Scenario: distributed system of electronic control units (ECUs) communicating over time-triggered bus

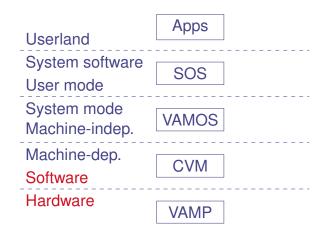


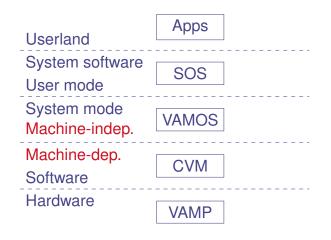
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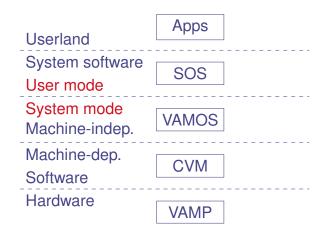


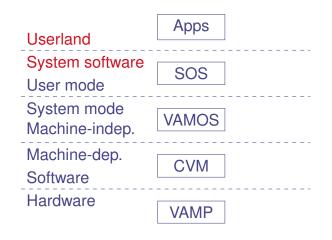
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- ! Clock synchronization and WCET analysis required

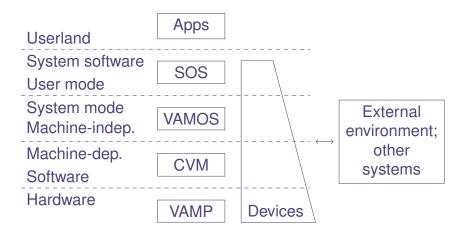




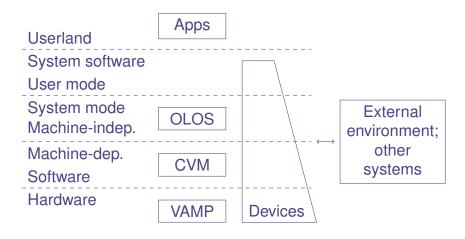








SP6 Automotive System:



Using appropriate formal specification & proof tools:

- 1. specify layers and languages used in the system
- 2. specify and verify algorithms used by the tool chain (or, alternatively, validate their output)
- 3. prove simulation statements between layers, arguing about the programs residing at the different layers

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All of this should enable to transfer correctness results for top-layer programs to their bottom-layer representation (~> obtain: verified stack).

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Computational Models

- Language models
 - Register-transfer language
 - Machine language, assembler
 - C0, a type-safe, Pascal-like subset of C

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 - DFAs modeling device behavior
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- Both types of models specified by next-state functions of the form $\delta(in, c) = (c', out)$ (small steps!)

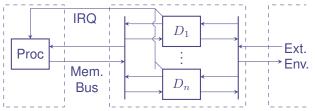
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· Build system / layer models from previous models

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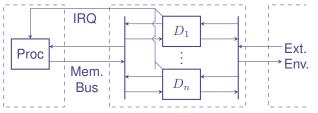
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Distributed models: connect via external environment

Semantics Stack for C0

 How to prove implementation of a layer correct wrt its model? Small-steps, concurrent semantics too cumbersome to use!

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Semantics Stack for C0

- How to prove implementation of a layer correct wrt its model? Small-steps, concurrent semantics too cumbersome to use!
- Stack of C0 semantics formalized in Isabelle/HOL
 - Machine-level small steps semantics (memory layout)
 - Small steps semantics
 - Big steps semantics
 - $^\circ\,$ Axiomatic semantics / C0 Hoare logics (with VCG)
- Layers in semantics stack related to each other via equivalence results
- \rightsquigarrow Use C0 Hoare logics for the bulk of verification work; integrate automatic proof tools into C0 Hoare logics.

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Example: Page Fault Handler Verification I

- Memory virtualisation via demand paging
- Implemented in C0 and assembler (swap access)

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Example: Page Fault Handler Verification I

- Memory virtualisation via demand paging
- Implemented in C0 and assembler (swap access)
- Verification of the C0 part
 - Verify in sequential C0 Hoare logics *enriched with* axiomatic semantics for swap memory access
 - Transfer down to the C0 big-steps level
 - Transfer down to the C0 small-steps level

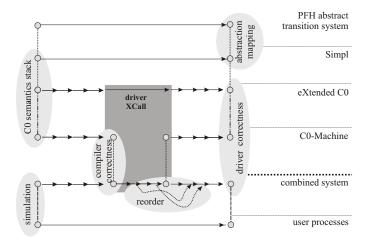
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 - Transfer down to the C0 big-steps level
 - Transfer down to the C0 small-steps level
- Verification of page in / out operations
 - Verify in assembler model with a hard disk
 - Generalize to model with other devices (trace reordering required!)
 - Wrap as C0 functions, verify wrapper (does not interfere with regular C0 small steps)

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Example: Page Fault Handler Verification II



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Repository Implementation and Structure

- Internally, we manage
 - documentations,
 - ° specifications,
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 - (proof) tools

of Verisoft project partners in a standard VCS. (\rightsquigarrow concurrent development, continuous integration and testing)

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• Everything is organized in *modules*, which have dependencies ('X needs / builds upon on Y').

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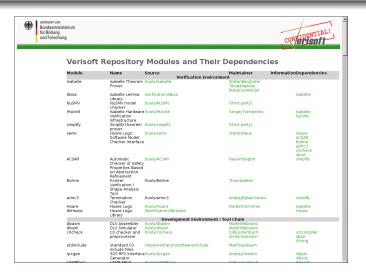
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Repository Realization



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• Goal: make stable, self-contained snapshots of non-confidential parts of the internal repository available publicly.

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- Goal: make stable, self-contained snapshots of non-confidential parts of the internal repository available publicly.
- Currently published:
 - Code verification of a doubly-linked list library
 - Code verification of a string library
 - Code verification of the Verisoft email client
 - Code verification of a big integer library
 - Code verification of the C0 compiler (includes: assembler and C0 small-steps semantics)

und Forschung	
Home	Verisoft Repository
Consortium Project Structure	In the Verisoft project, the formal pervasive verification of four exemplary computer systems, three of which come from the indus sector, is attempted. The layers, which are considered, range from the gate-level hardware over system software to communica and distributed applications.
Goals and Results	The Verisoft Repository allows to concurrently develop the many individual results that contribute to the overall verification results to manage them in a tractable manner.
 SP1: Methods and Tools SP2: Academic System 	In the repository, the artefacts developed by the project partners are being collected as modules and related to each other dependencies. Modules include documentations, specifications, implementations, proofs, and tools for development and verification
SP3: Correct Industrial	In the end, the repository must be self-contained: the set of modules for a given computer system under verification must allow
 SP4: Biometric Identification 	 to build an executable implementation or that system and to prove its top learn exercises.
System SP5: Project Management	Currently, substantial parts of the Verisoft theories and systems have been imported into the Verisoft repository and the reposito being used for further development.
 SP6: Automotive 	At this location, portions of the internal Verisoft repository that appear sufficiently stable and do not contain confidential dat industry partners, will be published.
Verisoft Repository	Publications
Publications	 vString-4-r11594.tar.gz (1.8M) — Code-Level Verification of a String Library (14 Dec 2006)
Press Contact	This release contains the code-level verification of a doubly-linked list library and a string library; the implementation language the C-like programming language C0. The verification is done in a Hoare-logic-based interactive software verifica environment for the therem proving environment fasbeller, which is also included.
	vemail-trunk-r15868.tar.gz (3.6M) — Code-Level Verification of an Email Client (18 May 2007)
Internal	This release contains the code-level warfscation of the small clerit of Subground: 2. Academic System relative to the serv provide by the simple operating system (SSD) and applications for signing and email transfer. The implementation language the Cike programming language CD. The verification is done in a Hoare-logic-based interactive software verifica environment for the theorem proving environment isabels.
 Auf Deutsch, Bitte! 	 vbigint-trunk-r19285.tar.gz (2.2M) — Code-Level Verification of a Big Integer Library (10 October 2007)
	This release contains the code-level verification of a big integer library used in Subprojet 2. Academic System and Subproje Biomatric indications system for the implementation of coptographic particles, the implementation language is the programming language (0. The verification is done in a Heart-Sogic-based interactive software verification environment for theorem provide environment tabelle.

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Verisoft Repository Publication: C0 Compiler Code Verification vc0compiler-trunk-r19956	
The Verisoft Project	
Verisoft is a long-term research project funded by the German Federal Ministry of Education and Research (bmb+f). Project managen Aerospace Center (DLR).	ent agency is the German
The main goal of the project is the pervasive formal verification of computer systems. Verisoft results (including implementations and appear sufficiently stable and do not contain confidential data di industry partners, are being published on the Verisoft web verification da compiler for a Calke language, contained herens, is the fourth relaxes of that kind.	formal correctness proofs) that page. The code-level functional
Overview	
Verifield's sub project 2 deals with the formal provates verification of a general-purpose computer system from gate-level has communicating paylications. At code is implemented in the programming language, col, which is a subsect of C. However, so there are at that Clinel. To allow execution of verified programs on the real hardware they must be compiled to branz code. This translates applications are emplemented in a high-weak programming language.	fication in Verisoft does not stop could itself introduce errors into
We have verified a simple non-optimizing C0 compiler. For pervasive verification it is not sufficient to have a verified code generation specification. We also need a verified compiler imperimentation in C0 excluding parsing phase or 10 operations) which allows us (all verified compiler binary on the target platform. After verifying the correctness of the compiling specification it is sufficient to show to produces the same code as the compiling specification.	ter boot strapping) to execute a
Here, we include only the compiler implementation and the corresponding correctness proofs. The correctness proof for the compili in an upcoming Verisoft repository release.	ng specification will be published
In addition to the compiler implementation, the implementation and verification of the additional libraries (for strings and lists) are al previous repository release (vString-4-r11594.tar.gz on the Verisoft Repository page) covering these verifications.	so included here; please see the
The verification of the complex implementation is done in a Hoare logic verification enconnent, which is implemented in the these purposes, the CO implementations in concrete syntable are translated in other Hoare logic representation the translation translate Based on this representation. In ware traples for total and partial connectiness are proven, supported by a verification condition perior the total concretes sensitio down of lower-lower sensition (, or, in the odd to the complex program running on the target architectus the total concretes sensitio down of lower-lower sensition (, or, in the odd to the complex program running on the target architectus the total concretes sensitio down of lower-lower sensition (, or in the odd to the complex program running on the target architectus the total concretes results down of lower-lower sensition (, or the odd to the complex program running on the target architectus the total concretes results down of lower-lower sensition (, or the odd to the complex program running on the target architectus the total concretes results down of lower-lower sensition (, the tend of lower lower sensition (, the lower lower lower) the complex program running on the target architectus to the lower lo	so part of this release (c0check). ator. Additionally, the absence of mong other things), to translate
As mentioned above, the verified implementation of the C0 compiler lacks a front-end and output routines. These are also implementation.	nented in the unverified c0check
The files in this release are placed in a number of directories, which we also call modules. The following graph lists the modules indicates the dependencies between the modules; the top-level module corresponds to the top-level results, i.e., the code verification	present in this release and also n of the CO compiler.
liverification	

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Overview

Versist's sub project 2 deals with the formal provative verification of a general-purpose computer system from gate-level hardware, to system software, and communicating gateliations. All code is implemented in the programming language CO, which is a subset of C levever, software verification in Versist dates not stop at the CO level. To allow security of the programs on the real hardware they musb be completed to brany code. This translation code with the subset of the provided to brany code and the code of the provided to brany code. This translation code with introduce errors into a policitations are interested in a hardware they musb be completed to brany code. This translation code with introduce errors into a spontaneous system vertication when the system software and applications are interested in a hardware thore programming language.

We have verified a simple non-optimizing C0 compiler. For pensates verification it is not sufficient to have a verified code generation algorithm (also called compiling specification). We also need a verified compiler implementation in C0 (selution) parsing phase or (to Operation) which allows us (after boot transping) to execute a verified compiler binary on the target platform. After verifying the correctness of the compiling specification it is sufficient to show that the compiler implementation produces the same code as the compiling specification.

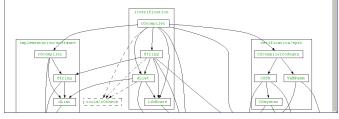
Here, we include only the compiler implementation and the corresponding correctness proofs. The correctness proof for the compiling specification will be published in an upcoming Verisoft repository release.

In addition to the compiler implementation, the implementation and verification of the additional libraries (for strings and lists) are also included here; please see the previous repository release (vString-4-r11594.tar.gz on the Verisoft Repository page) covering these verifications.

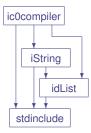
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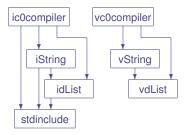


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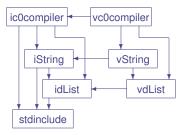
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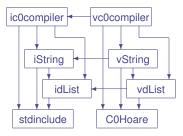
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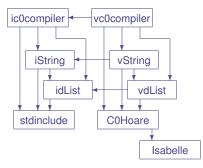
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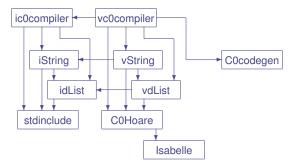
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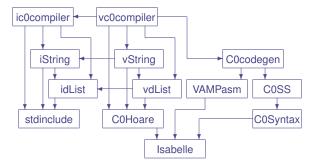
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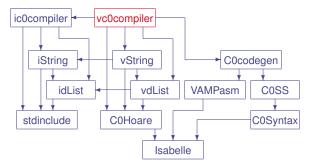
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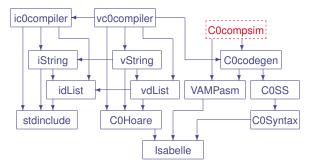


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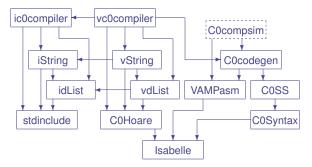
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- Theorem: Generated code simulates C0 computation (part of an upcoming Verisoft repository release)
- To use that theorem (e.g., bootstrap): more nodes...

Conclusion

- Verisoft: verification of entire systems of industrial interest
- System verification environment / repository:
 - ° Contains all artifacts needed for the verification
 - Architecture largely determined by structure of implementation and its tool chain
- Two verified stacks:
 - computational models (often concurrent, small steps)
 - semantics (increase verification productivity)
- Repository snapshots: www.verisoft.de

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