

Simulation vs. Formal:

"Absorb what is useful; reject what is not."

Briggs Lee

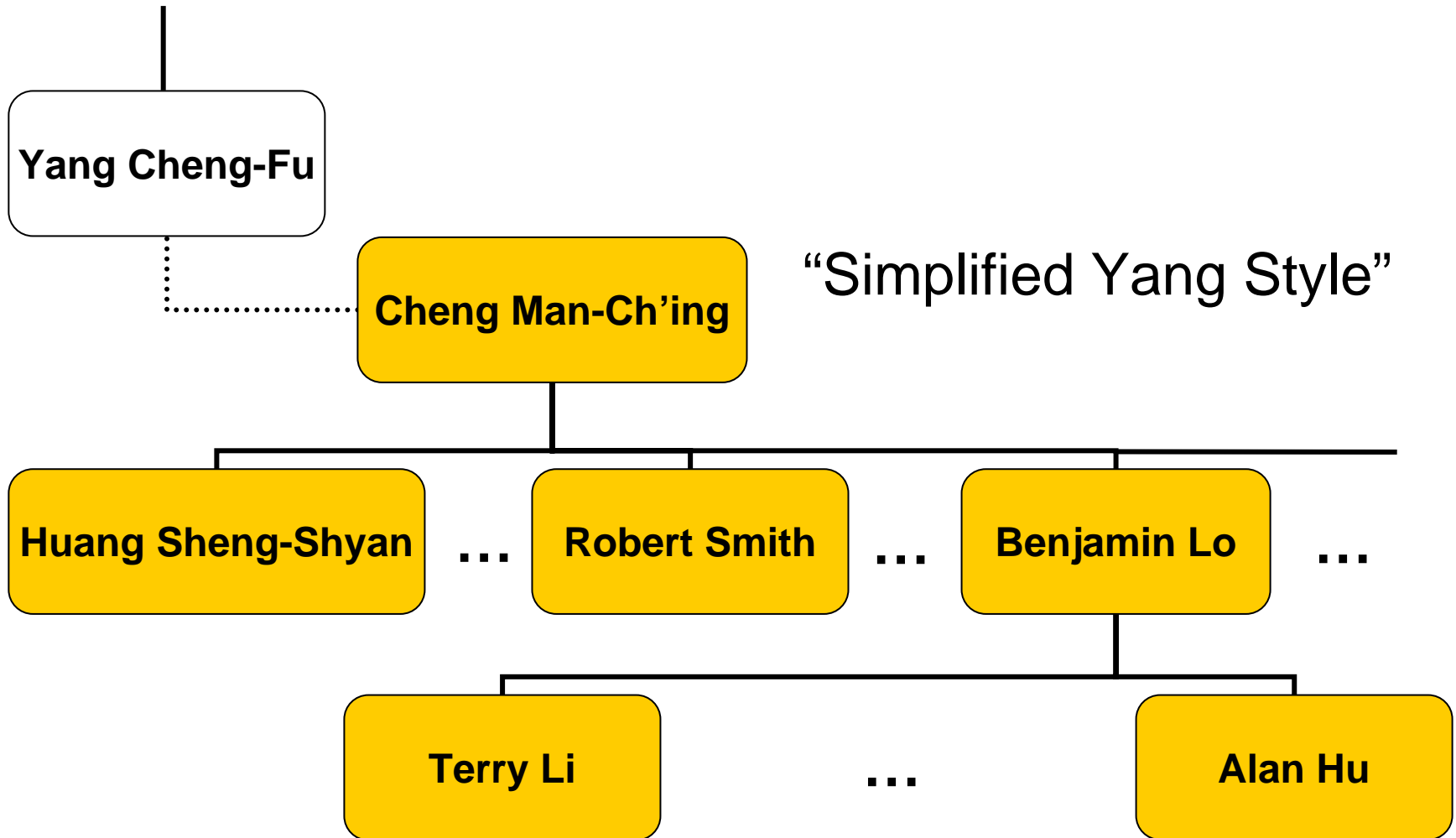
Alan J. Hu

University of California

Approach to
Verification

Absorb what is useful.
Reject what is useless.
-- Bruce Lee

My T'ai Chi Ch'uan Genealogy



Characteristics of Traditional Martial Arts Instruction

- Study in a school led by the master.
- Introductory classes are in groups, with syllabus set by the master.
- Advanced study is one-on-one with master.
- Interact almost exclusively with fellow students and the master.
- Travel to tournaments/workshops. Compete/interact with others of same style.
- Read books, articles, papers by masters of your own style.
- Denigration of other styles.

Problem?

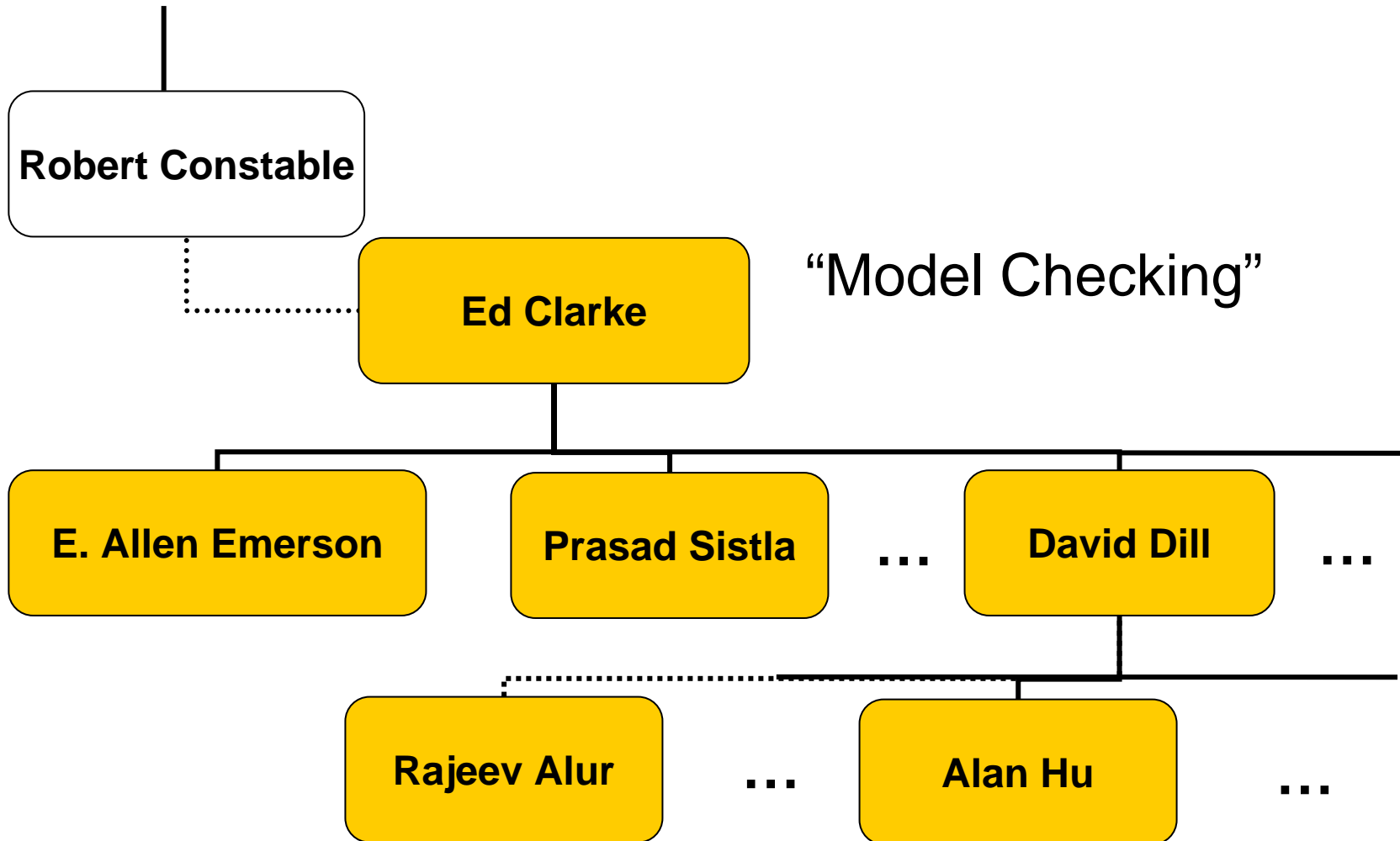
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Characteristics of Traditional EE/CS Instruction

- Study in a school led by the professors.
- Introductory classes are in groups, with syllabus set by the professor.
- Advanced study is one-on-one with professor.
- Interact almost exclusively with fellow students and the professor.
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My Verification Genealogy



Problem?

- Slow spread of good ideas
- Failing to notice one's own assumptions, blind spots

Formal vs. Simulation

- Exhaustiveness

- Scalability

Formal vs. Simulation

■ Exhaustiveness



```
graph TD; A([Exhaustiveness]) --> C(?); B([Scalability]) --> C;
```

The diagram consists of two red ovals at the top. The left oval contains the text '■ Exhaustiveness' and the right oval contains '■ Scalability'. From the bottom of each oval, a red arrow points downwards towards a large black question mark centered between the two arrows.

■ Scalability

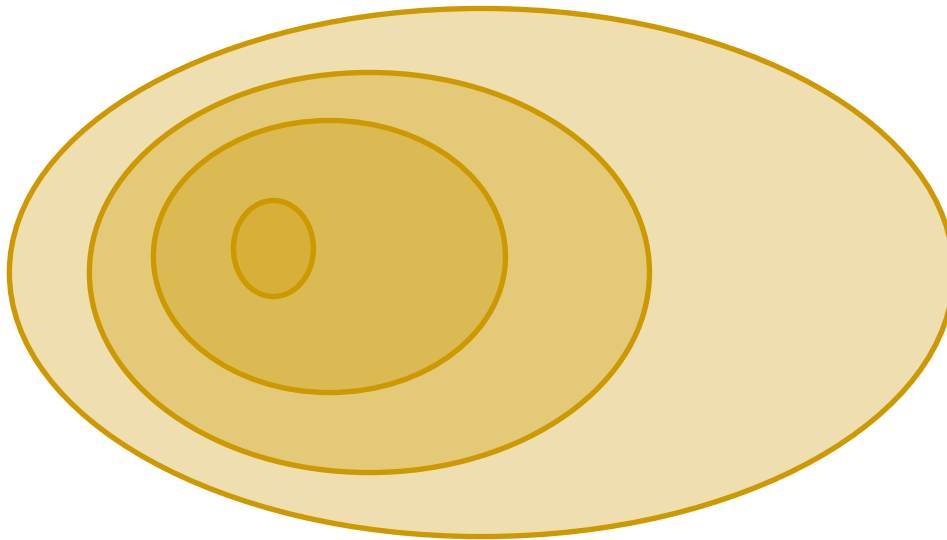
?

Mixing Formal and Simulation

- Methodological Combination:
 - Use formal wherever it can work.
 - Everywhere else, simulate.
- Semi-Formal:
 - Use a bit of formal while simulating.
 - Under-approximate images during formal verification.

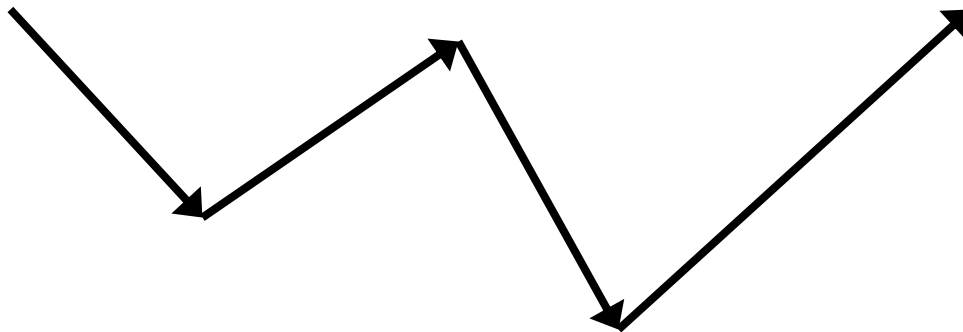
Semi-Formal: 1st Generation

- Formal (Symbolic Model Checking):



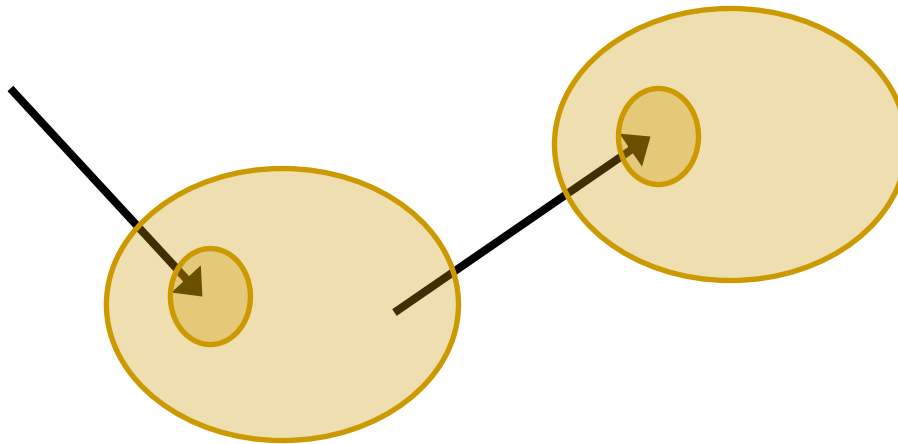
Semi-Formal: 1st Generation

- Dynamic Verification (Simulation/Emulation):



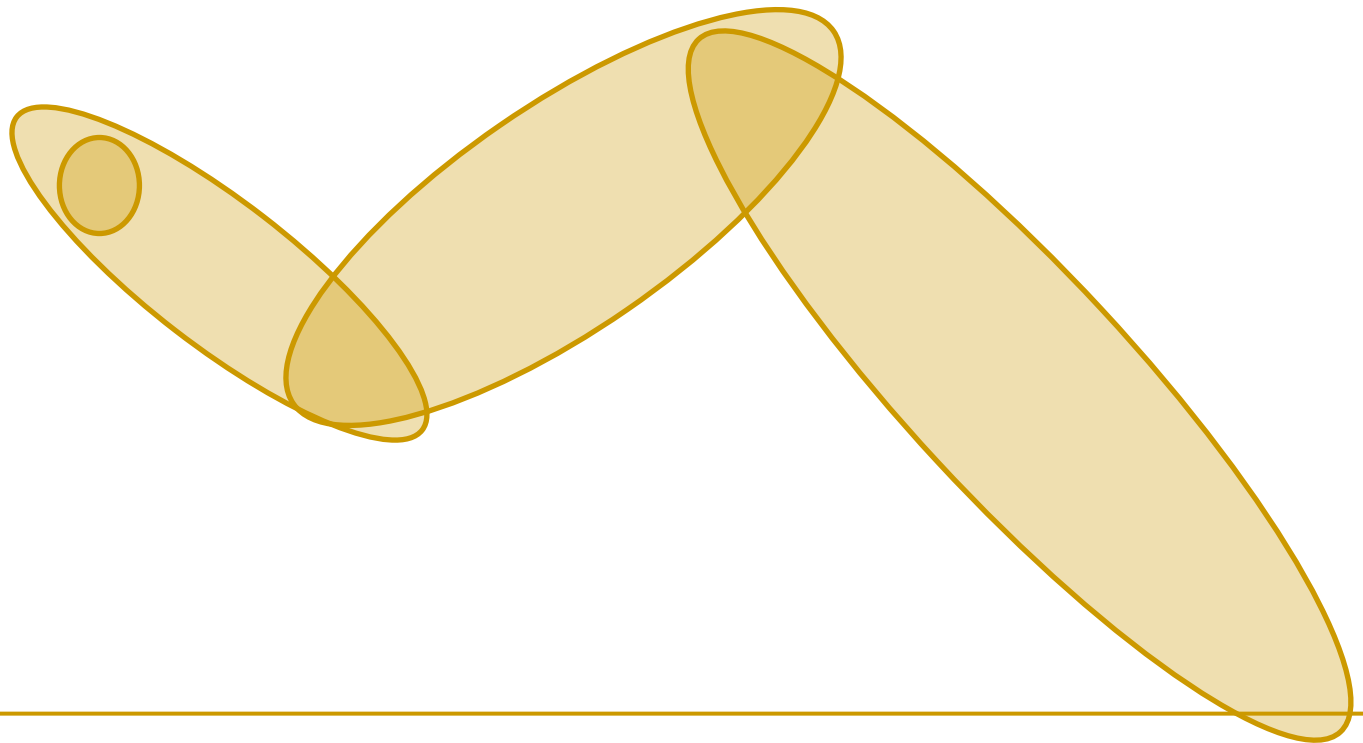
Semi-Formal: 1st Generation

- Semi-Formal (a bit of formal while simulating):



Semi-Formal: 1st Generation

- Semi-Formal (Under-Approximate Images):



Formal vs. Simulation

- Exhaustiveness
- Scalability

Formal vs. Simulation

- Exhaustive analysis is useful!
 - Smart, brute force (BDDs, SAT, SMT, etc.)
 - Abstraction
- Scalability
- Machine-readable specifications.

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E.g., Constrained Test Generation

- Machine-readable specifications.

Formal vs. Simulation

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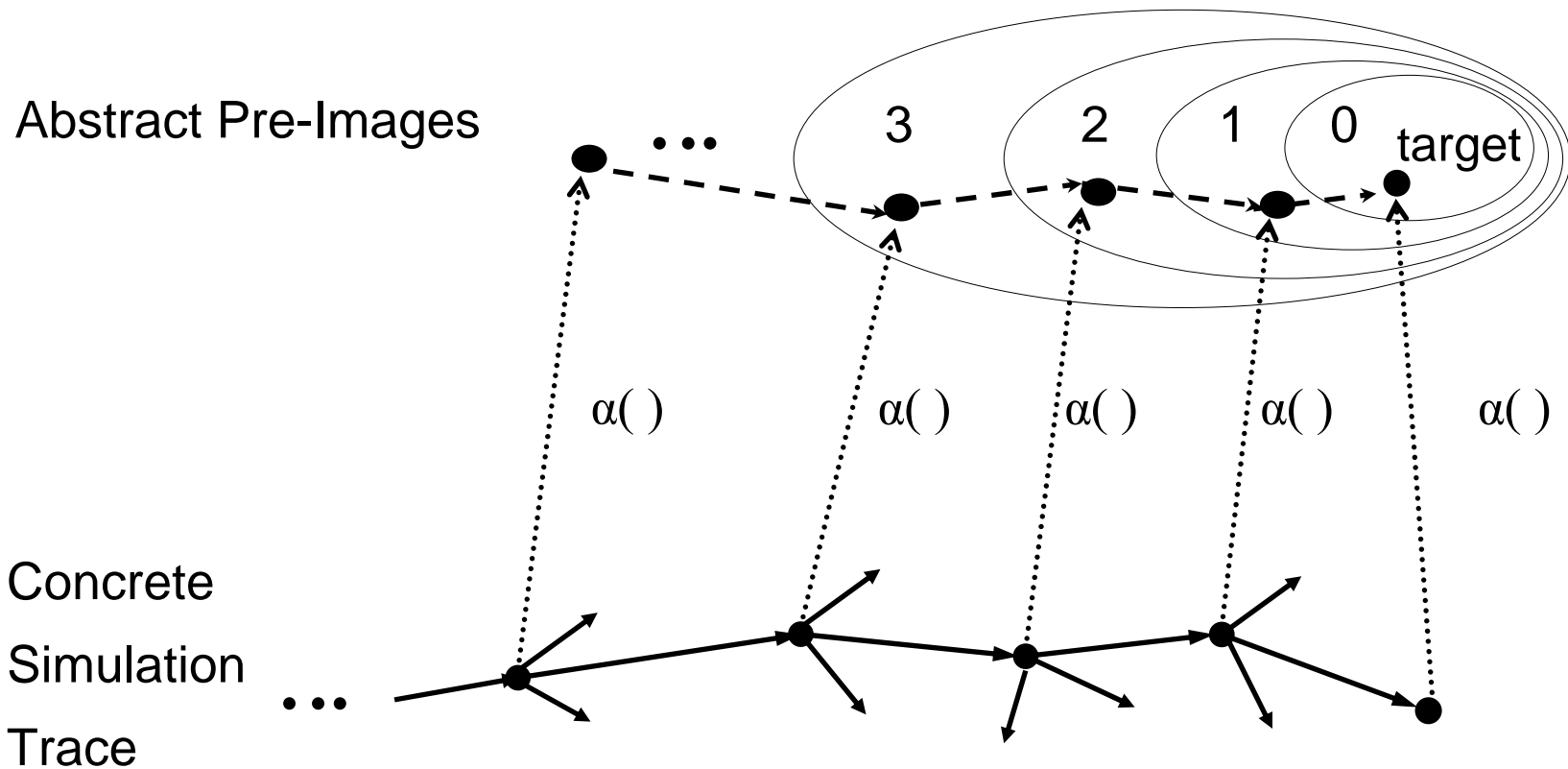
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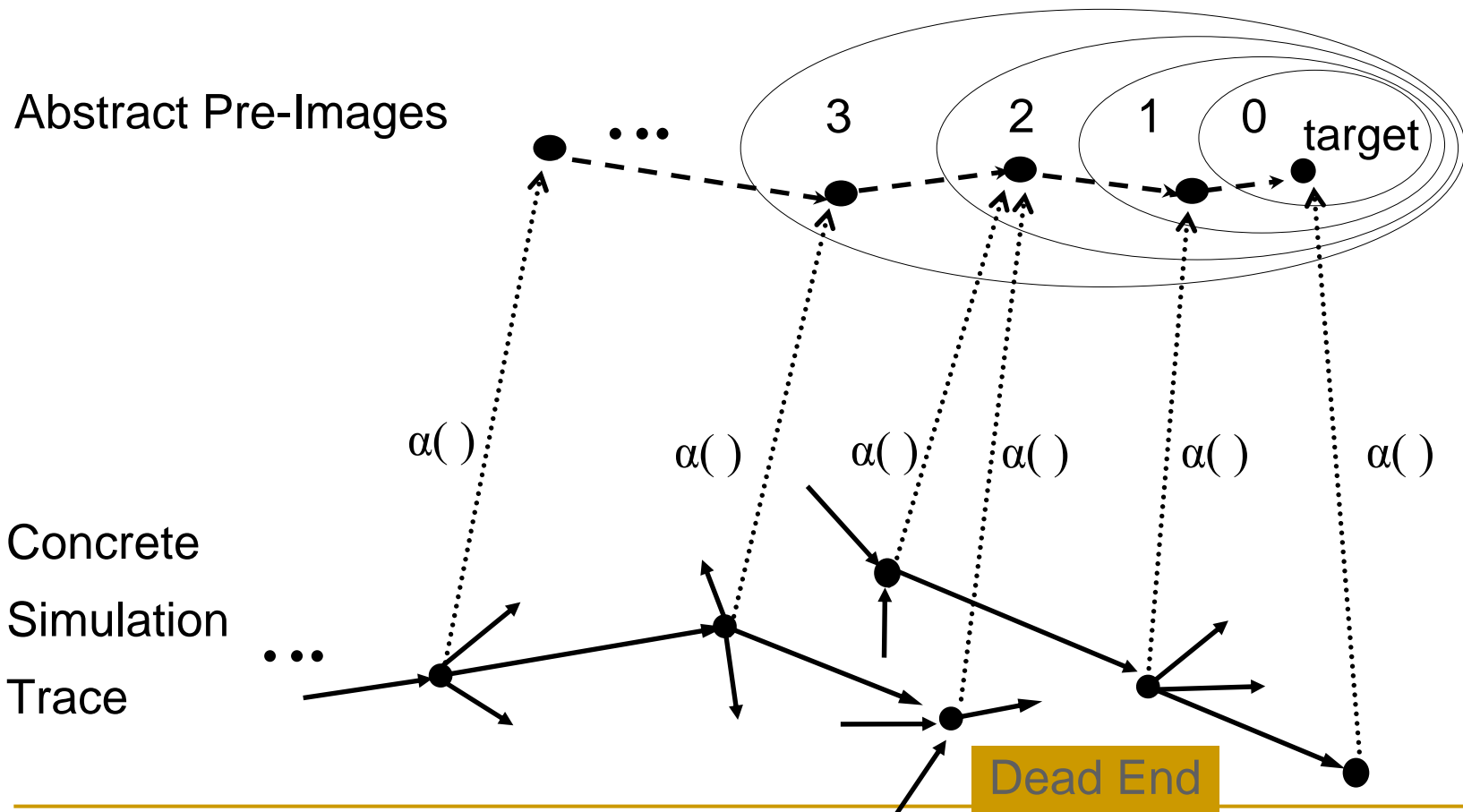
E.g., Abstraction-Guided Simulation

- Machine-readable specifications.

Abstraction-Guided Simulation



Leaky Abstractions



Formal vs. Simulation

- Exhaustive analysis is useful!

- ☐ Smart, brute force (BDDs, SAT, SMT, etc.)
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E.g., Abstraction-Guided Simulation

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E.g., Assertion-Based Verification

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- Scalability
 - Compiled code -- Execute. Don't interpret.
- Metrics
- Domain Expertise

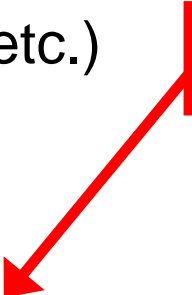
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- ```
graph LR; A[Domain Expertise] --> B[Smart, brute force (BDDs, SAT, SMT, etc.)]; A --> C[Abstraction]; A --> D[Machine-readable specifications];
```

# Formal vs. Simulation

- Exhaustive analysis is useful!
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  - Domain Expertise
- E.g., Coverage for Formal Specs
- 

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E.g., Predicate Complete Testing

# Predicate Complete Testing

- Predicate Abstraction: Use a set of  $n$  predicates as abstraction function.

$$\alpha : C \rightarrow B^n$$

- Heuristic: Use all conditions in program as predicates.
- Predicate Complete Testing: Use the abstract state space as coverage metric for simulation.

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E.g., SATOMETER,  
Semi-Formal BMC

# SATOMETER, Semiformal BMC

- SAT solvers use learned clauses to track how much of the solution space has been explored.
- Collect these clauses in a ZBDD.
- Report fraction to user.

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# Maximizing Processor Performance

- Anything that reduces instruction-level parallelism costs performance:
  - Control Dependence – Branch mispredict penalty 10-20 cycles.
  - Data Dependence – L2 miss penalty 50-100 cycles.
- Unpredictable branch costs 10s of instructions.
- Random memory access costs 100s of instructions.
- Parallelizable instructions are free.

# Compiled Code Simulation

## ■ Conventional Logic Simulator:

- ❑ Stores circuit in memory
- ❑ Walks that data structure
- ❑ Interprets gates/operators
- ❑ Hundreds of instructions per gate.

## ■ Compiled Code Simulator:

- ❑ Compiles circuit into machine instructions.
- ❑ Executes those instructions. No interpretation.
- ❑ Few branches. Fewer memory accesses.
- ❑ A few instructions per gate.

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E.g., SATOMETER,  
Semi-Formal BMC

# Conventional SAT Solver for BMC

- SAT solver stores circuit (as clauses) in memory.
- SAT solver walks this data structure.
- SAT solver interprets clauses.
- Even values on wires are encoded into data structure.
- Poor performance! (90% of time is BCP.)



# Compiled Circuit SAT Solver

- Compile verification problem into a program.

- Brute Force:

```
while (vector = pick_a_vector()) {
 if (compiled_simulate(vector))
 return SAT;
 record_unsuccessful_trial(vector);
}
return UNSAT;
```

# Compiled Circuit SAT Solver

- Compile verification problem into a program.

- New Idea:

```
while (vector = pick_a_vector()) {
 if (smart_compiled_simulate(vector))
 return SAT;
 record_unsuccessful_trial(vector.learned);
}
return UNSAT;
```

# Compiled Circuit SAT Solver

- It sometimes works great.
- E.g.,  $2n$  by  $n$  bit Radix-2 SRT divider.

| n | Chaff  | Compiled     |
|---|--------|--------------|
| 4 | 1.2    | 0.4          |
| 5 | 7.5    | 4.7          |
| 6 | 98.1   | 56.8         |
| 7 | 2848.4 | 735.2        |
| 8 | time   | time(0.7737) |

- Also reports progress made.
- (Published as “Semiformal Bounded Model Checking”)

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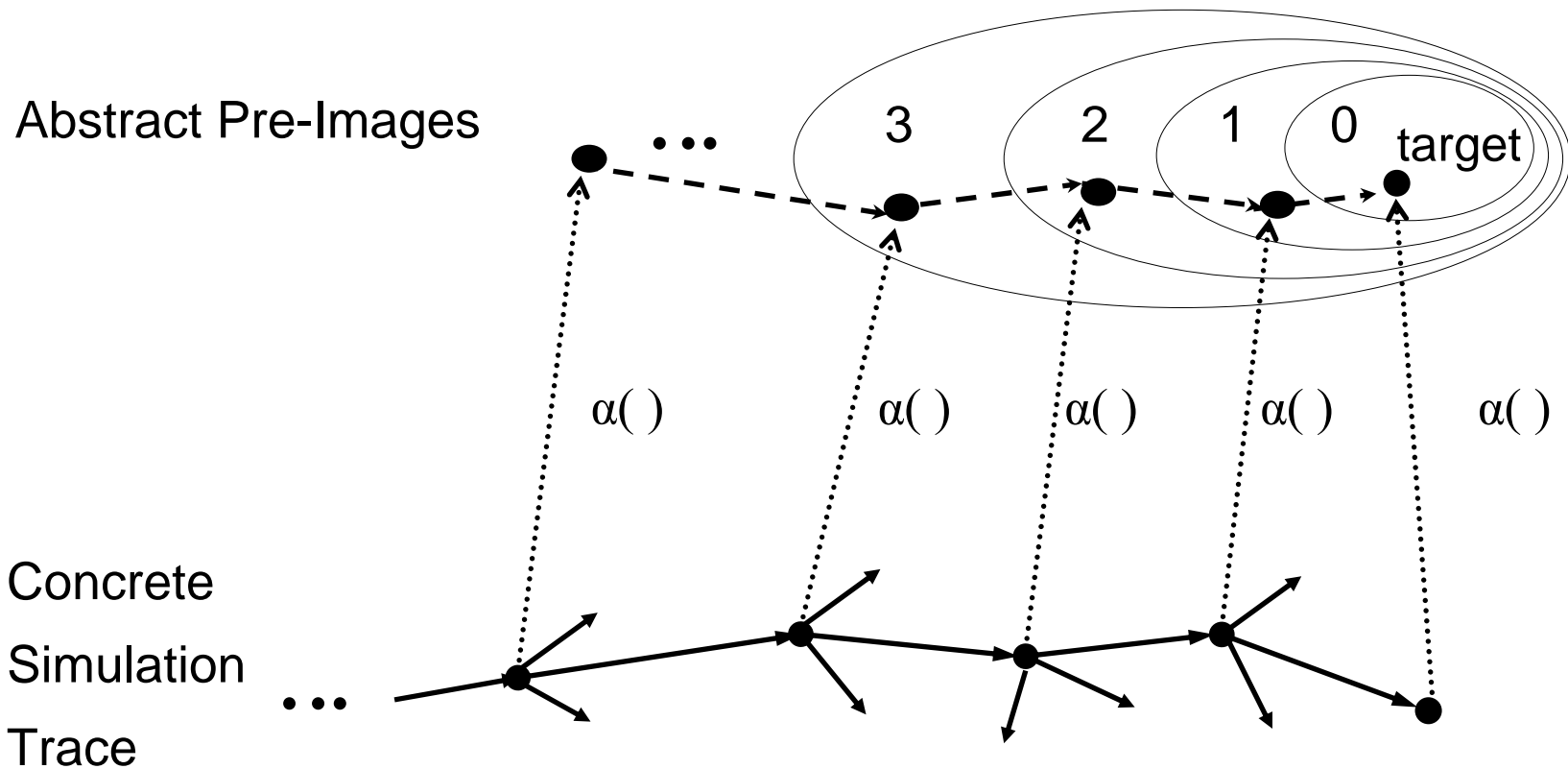
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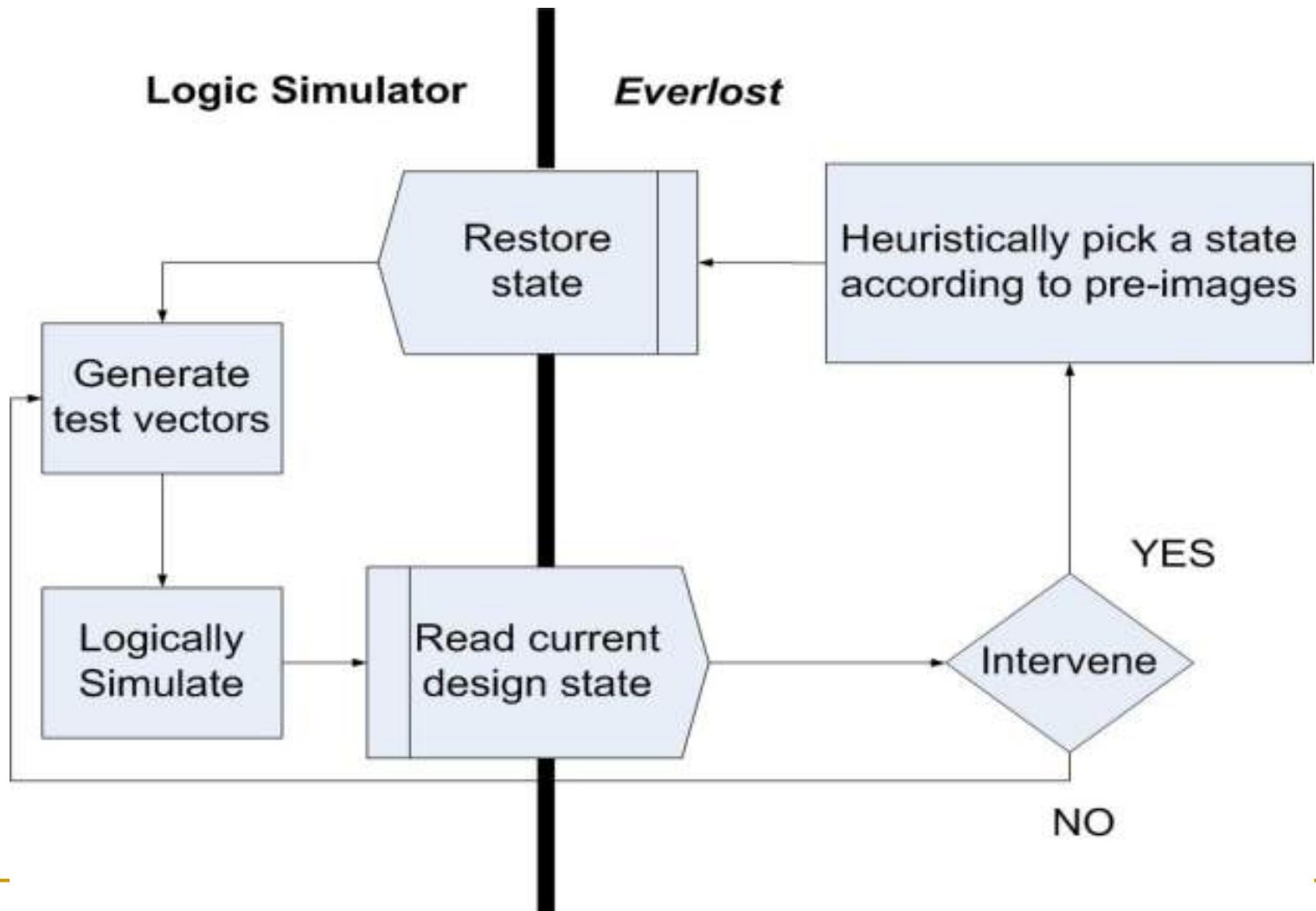
- Domain Expertise

E.g., EverLost

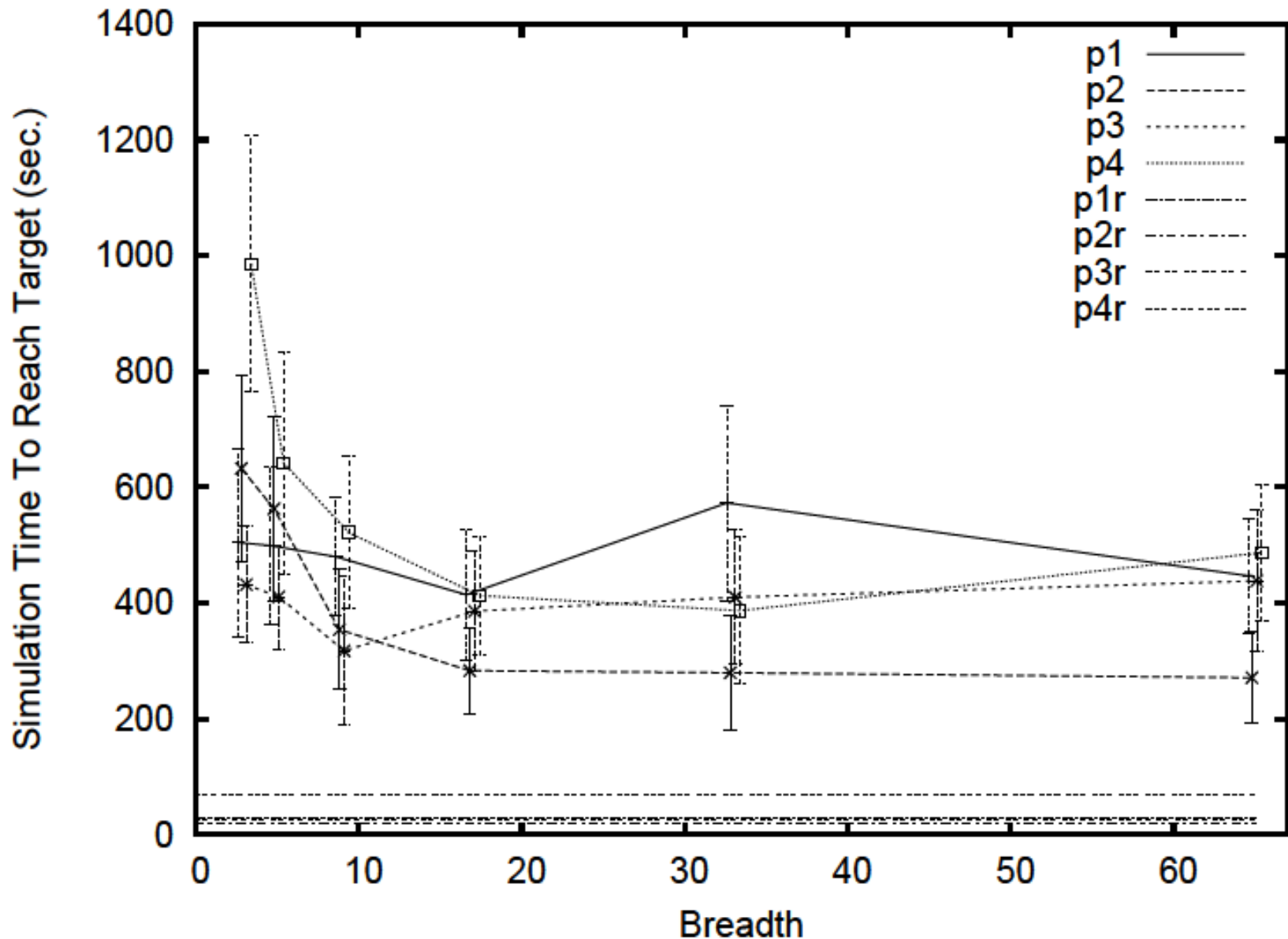
# Abstraction-Guided Simulation



# Platform: EverLost

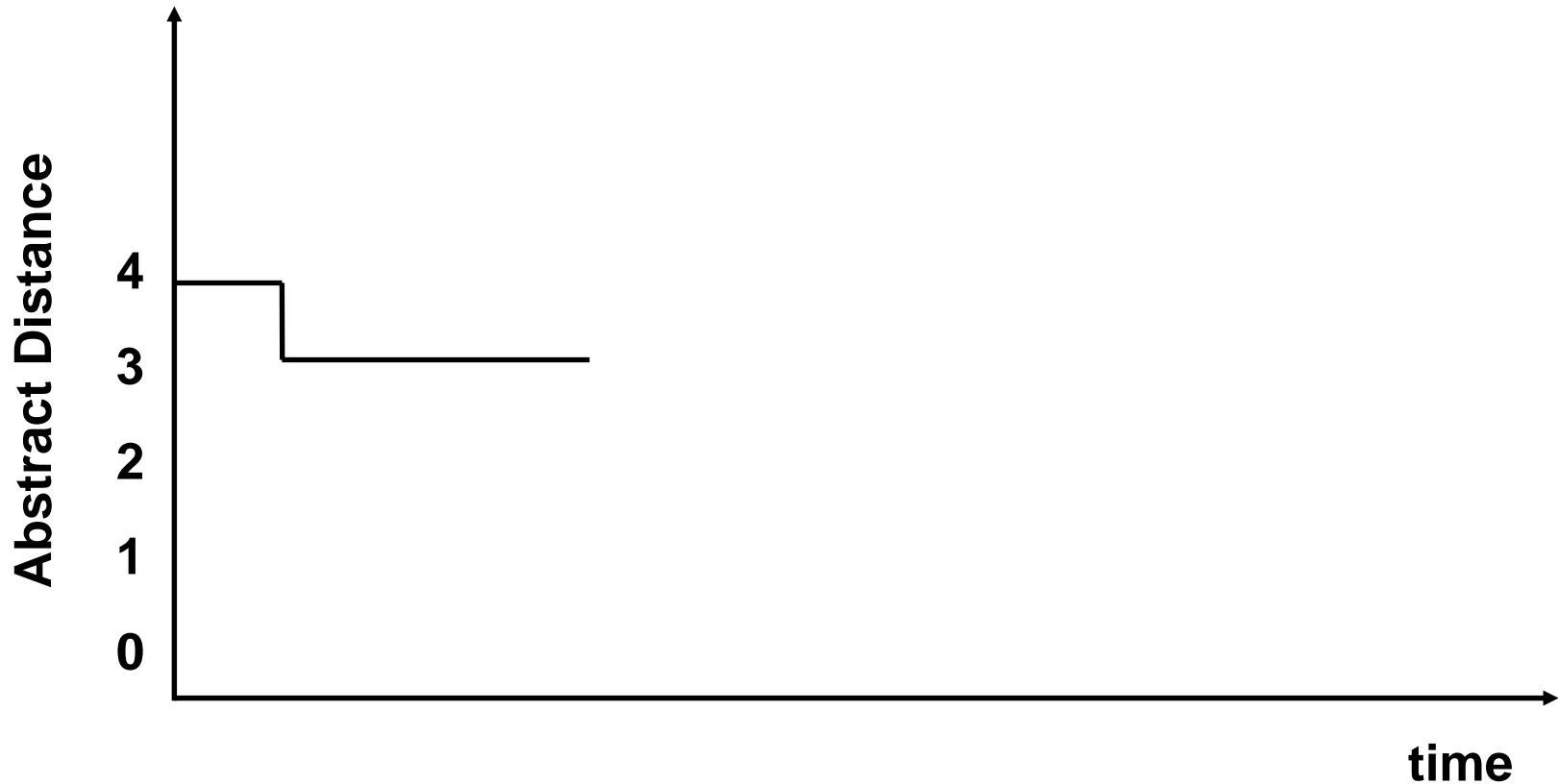


# Simulation Time for SimSearch

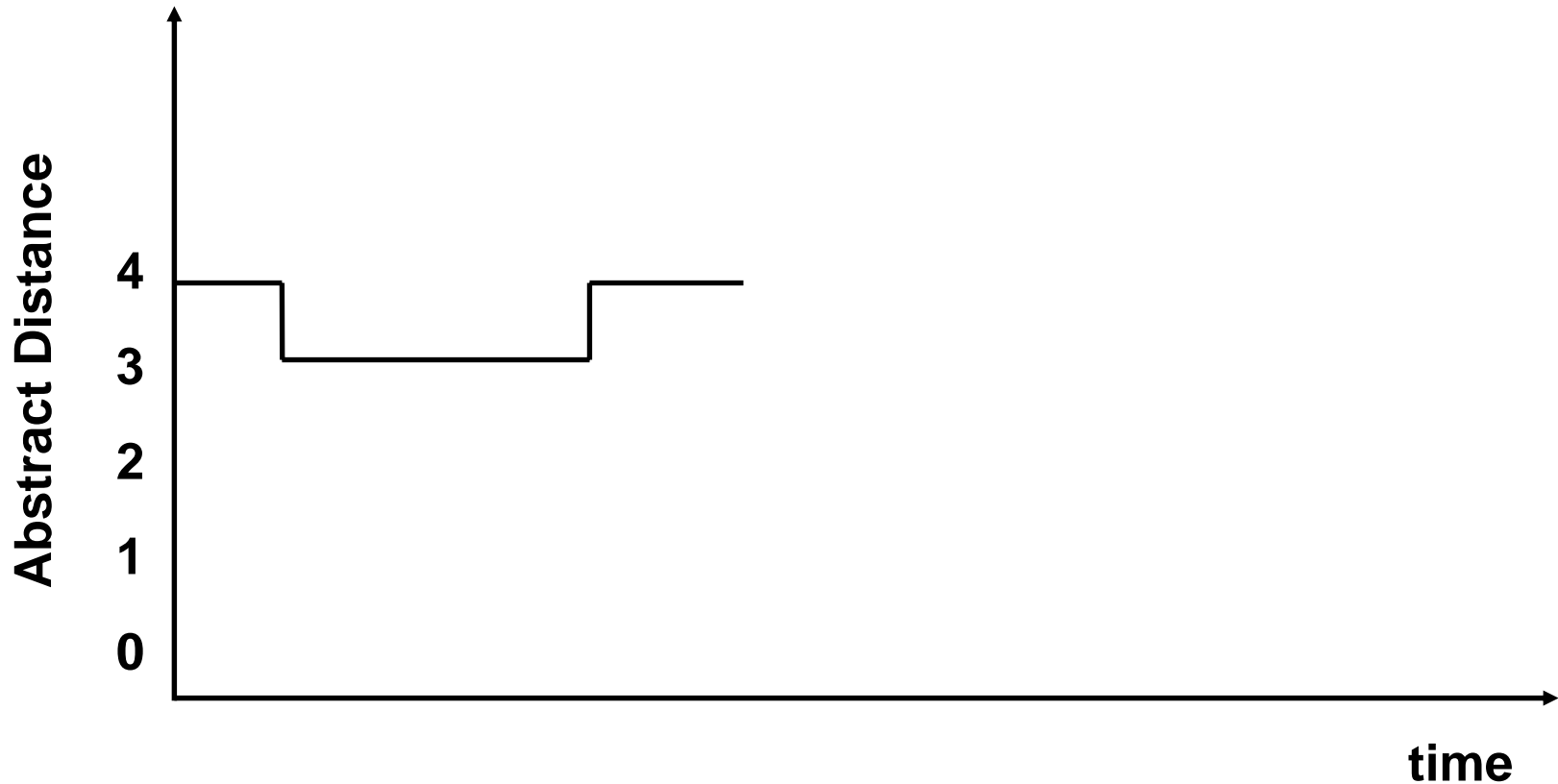




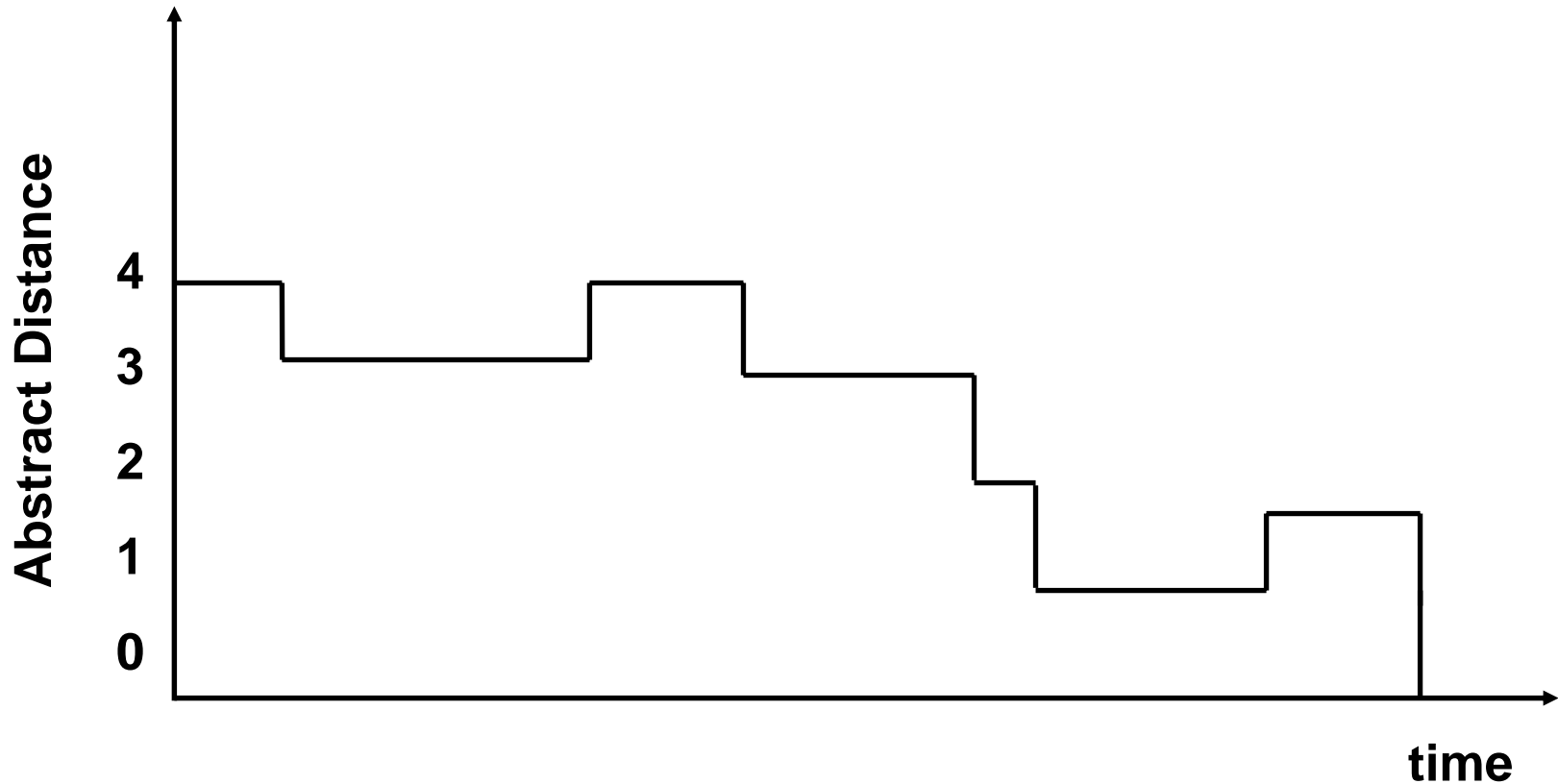
# Simulation Trace: Expected Results



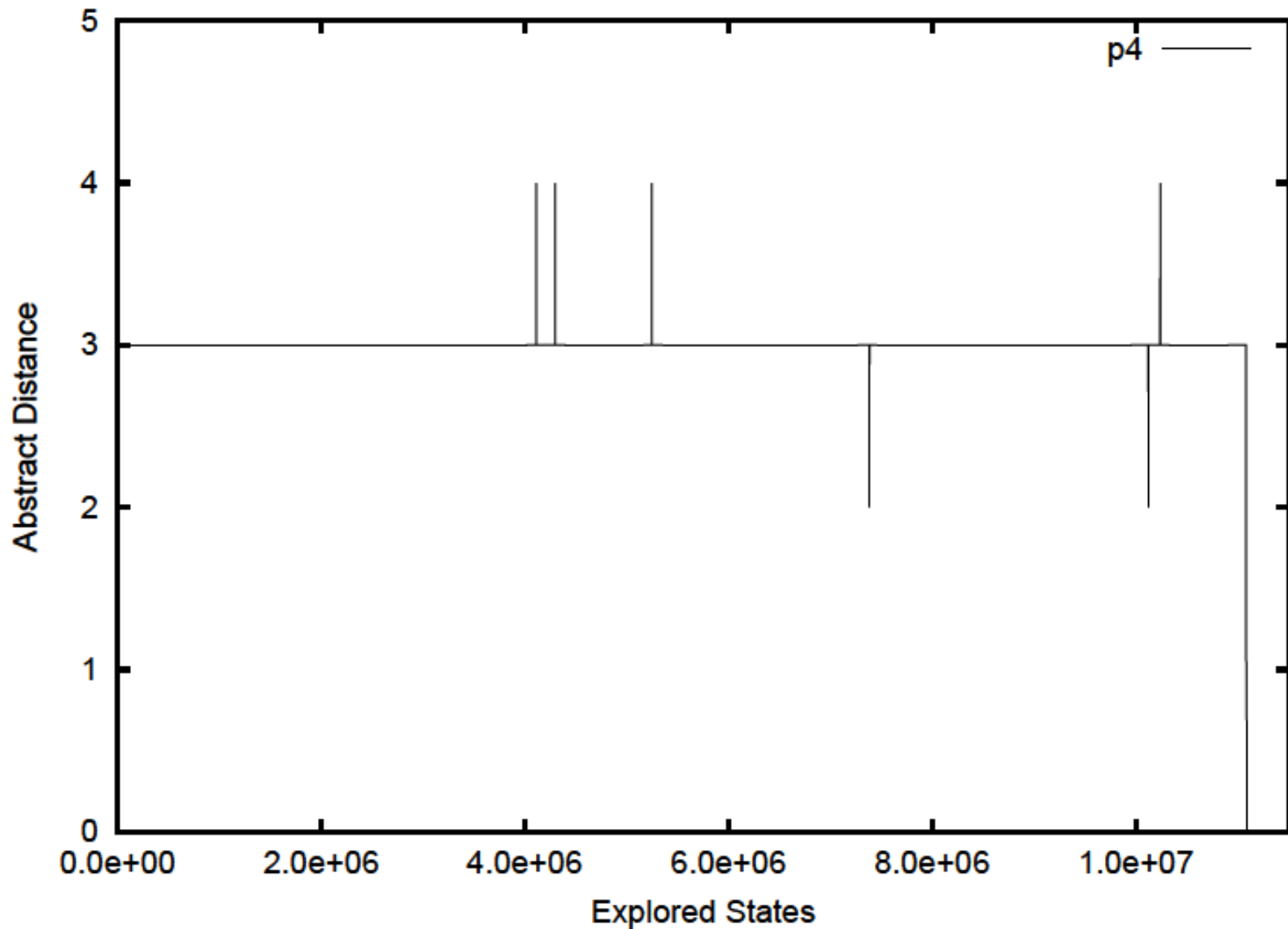
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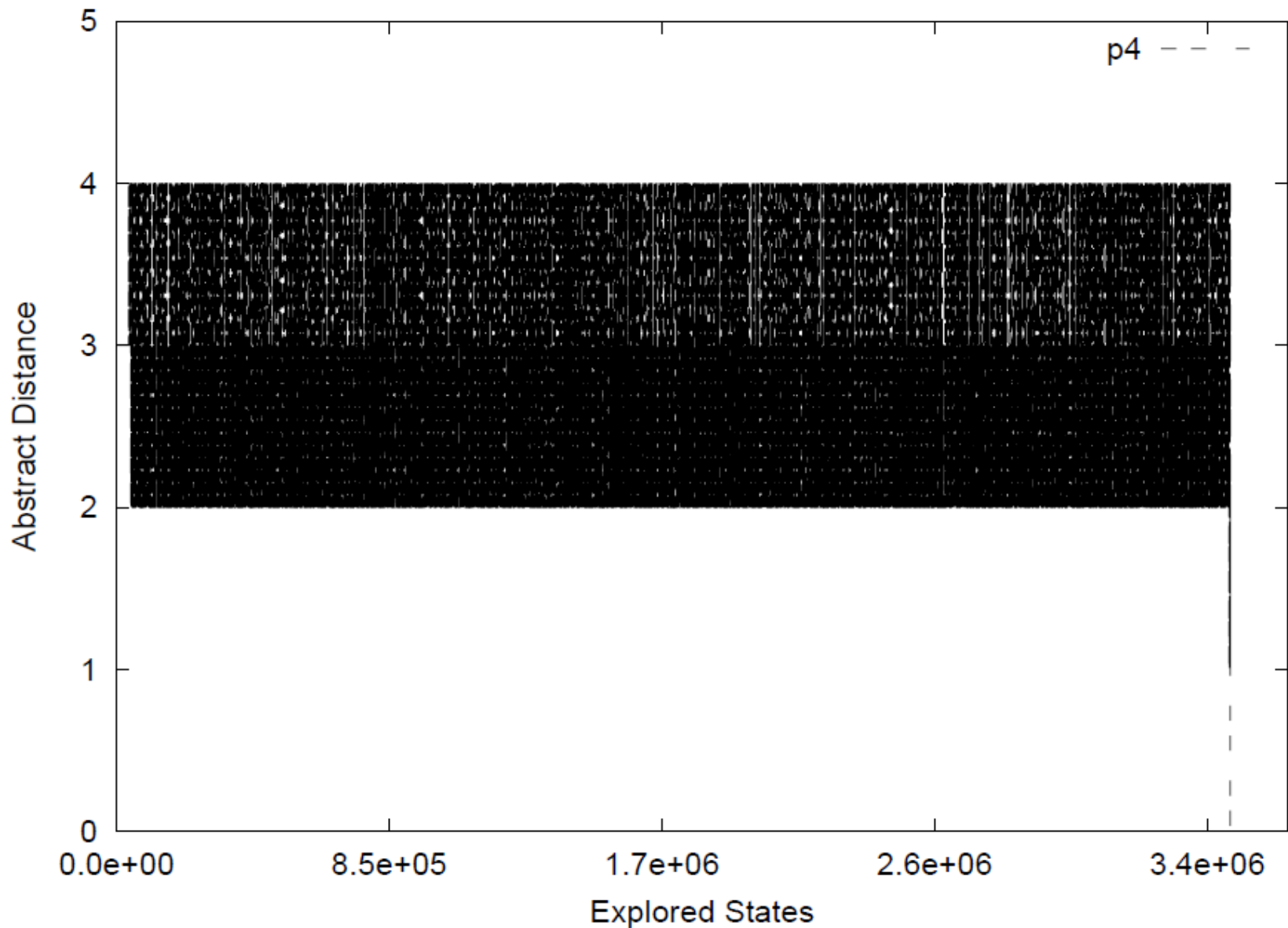
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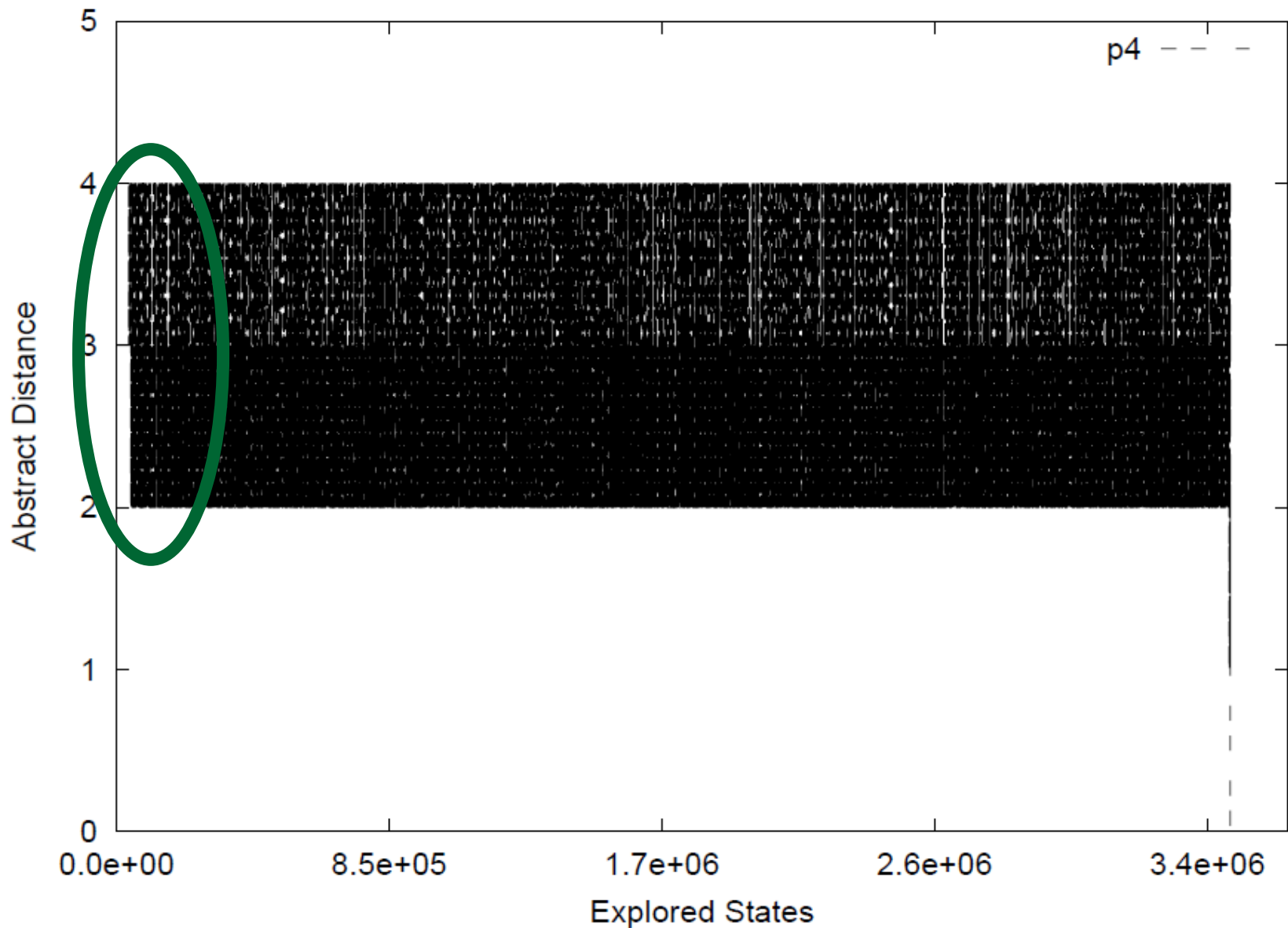
# Hard Gains, Easy Losses



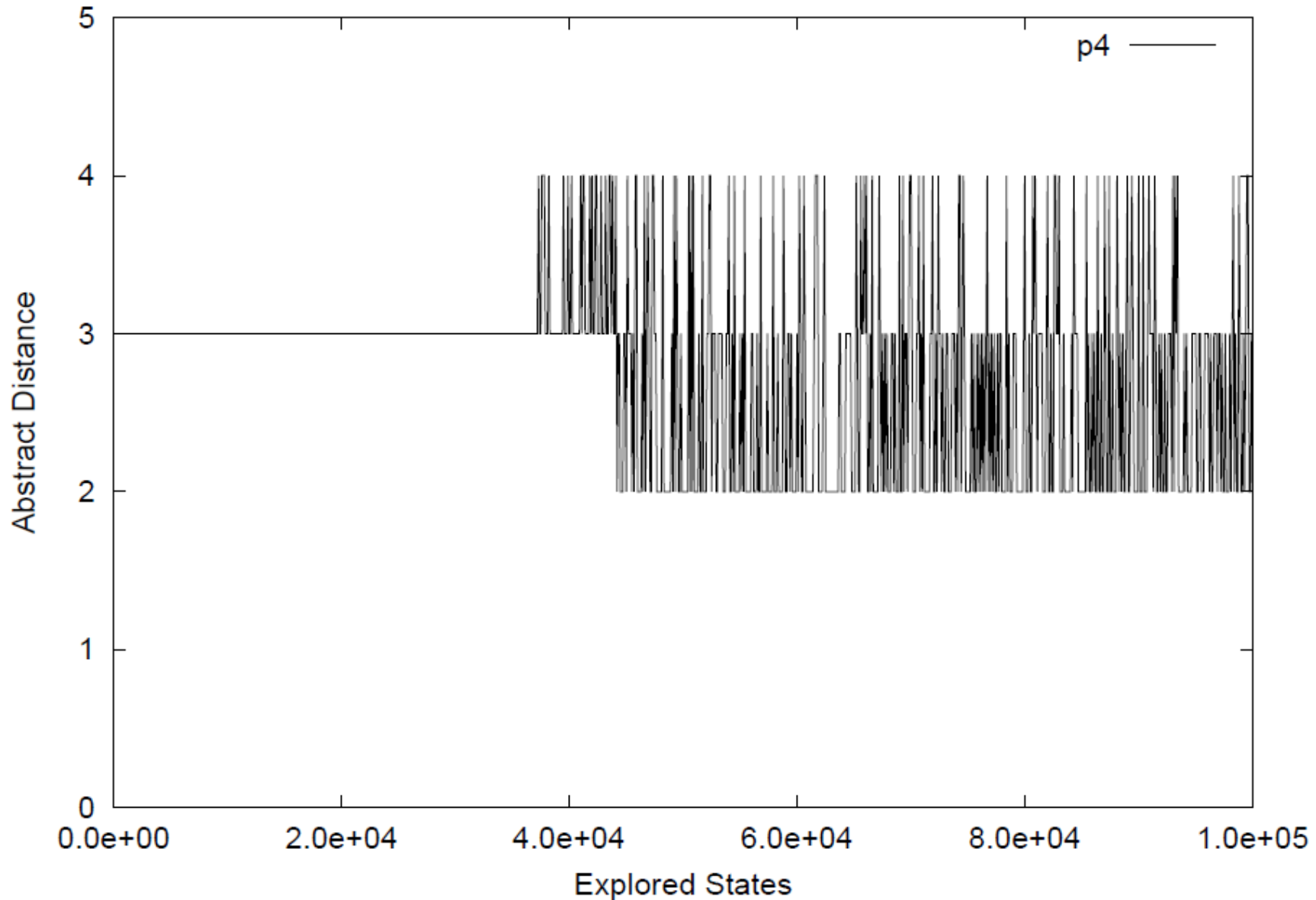
# Simulation Trace for New



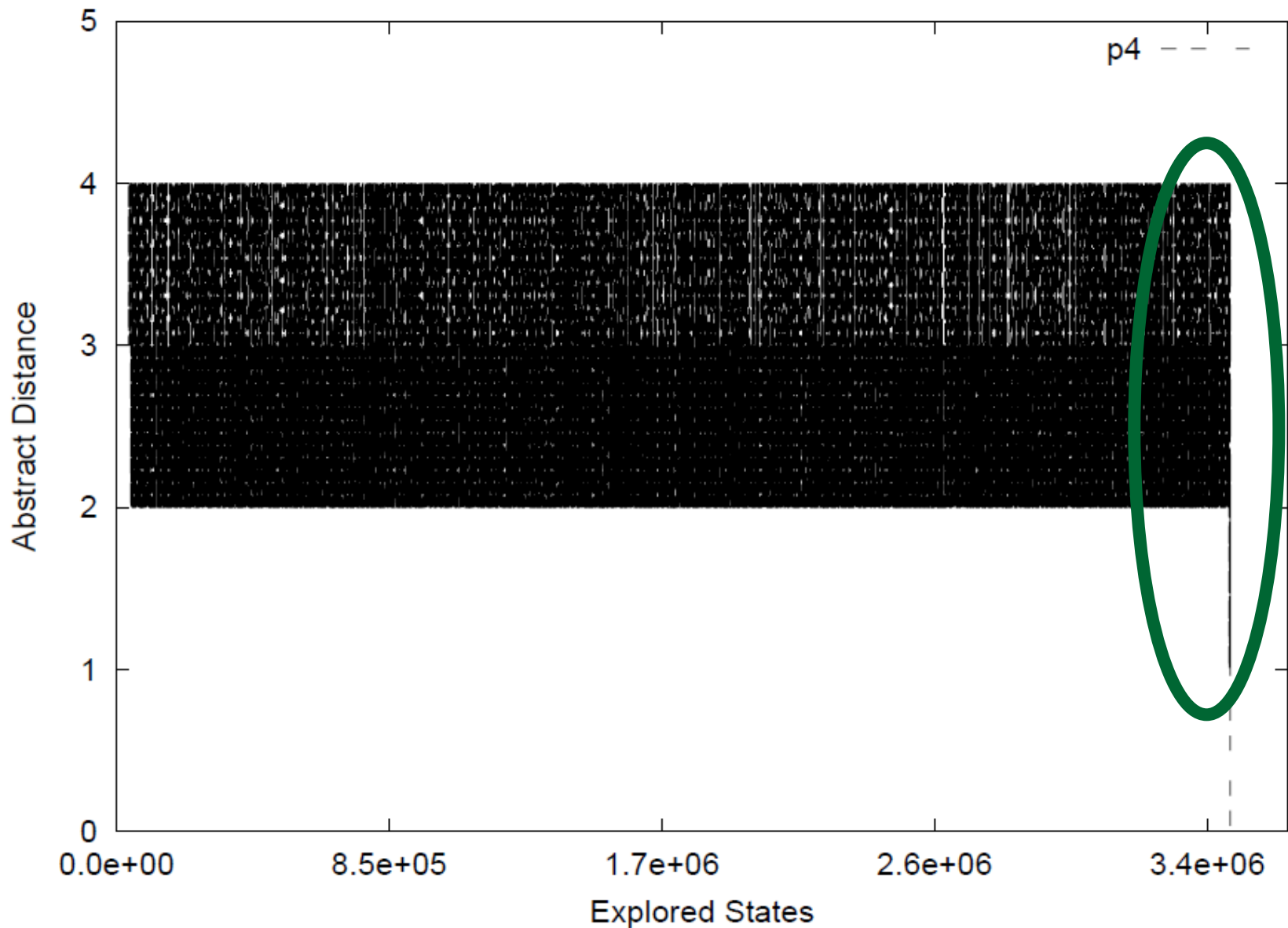
# Simulation Trace for New



# Enlarging Simulation Trace

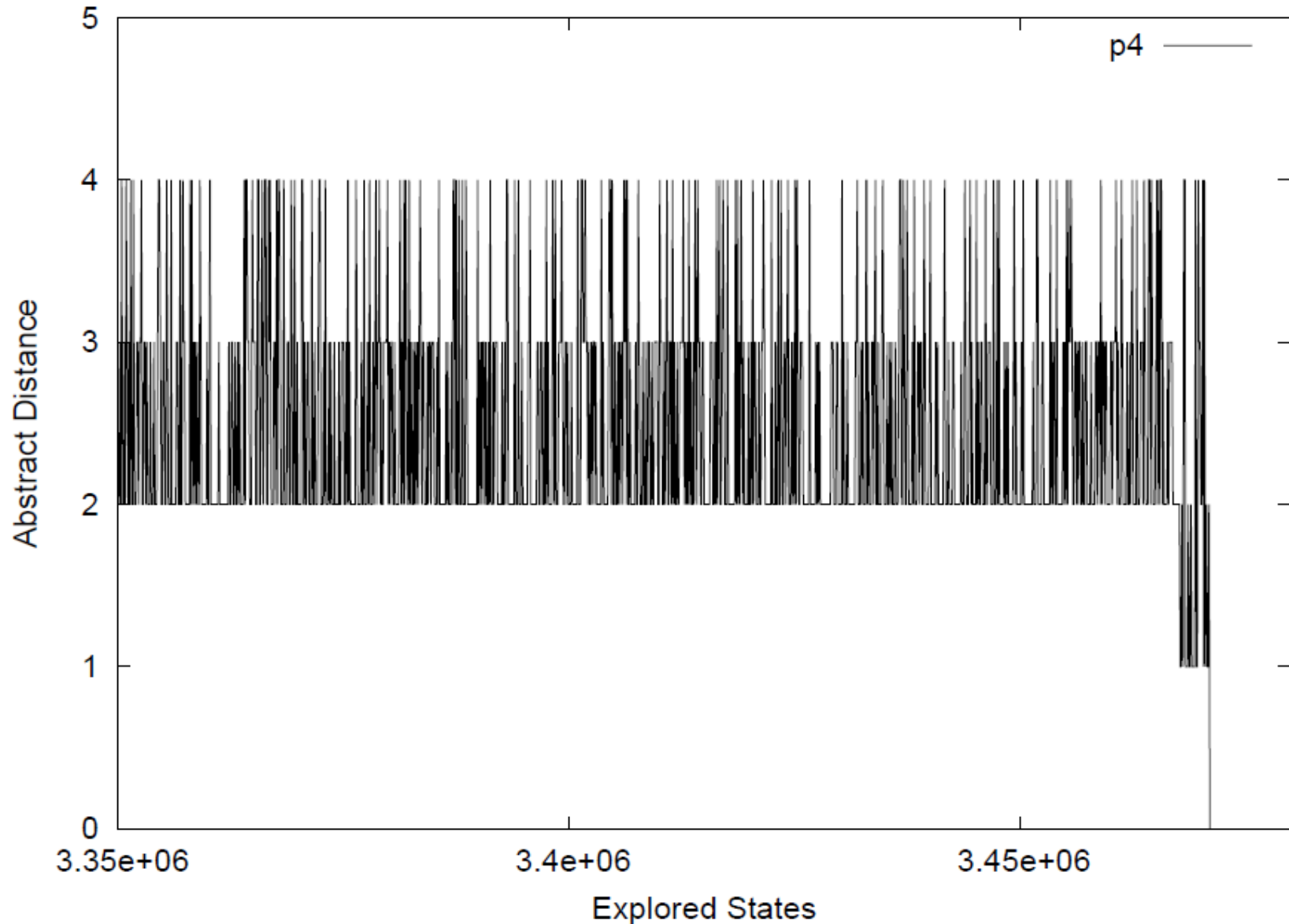


# Simulation Trace for New





# Enlarging Simulation Trace



# Random vs. Guided: p0

| Run | Min<br>(sec) | 95% Confidence Interval |                  |               | Max<br>(sec) |
|-----|--------------|-------------------------|------------------|---------------|--------------|
|     |              | Low<br>(sec)            | Average<br>(sec) | High<br>(sec) |              |
| R   | 27.5         | 656.8                   | 1011.3           | 1365.8        | 3999.3       |
| G   | 0.4          | 1.2                     | 1.4              | 1.7           | 2.9          |

# Random vs. Guided: p1

| Run | Min<br>(sec) | 95% Confidence Interval |                  |               | Max<br>(sec) |
|-----|--------------|-------------------------|------------------|---------------|--------------|
|     |              | Low (sec)               | Average<br>(sec) | High<br>(sec) |              |
| R   | 106.8        | 2224.2                  | 3,510.1          | 4,795.9       | 10885.5      |
| G   | 150.8        | 4015.6                  | 6,681.6          | 9,347.7       | 28865.0      |

# Random vs. Guided: p2

| Run | Min<br>(sec)                     | 95% Confidence Interval |                  |               | Max<br>(sec) |
|-----|----------------------------------|-------------------------|------------------|---------------|--------------|
|     |                                  | Low<br>(sec)            | Average<br>(sec) | High<br>(sec) |              |
| R   | Timed Out (>100hrs) 22/22 Trials |                         |                  |               |              |
| G   | 481                              | 6,110                   | 10,586           | 15,061        | 51,444       |

# Random vs. Guided: p3

| Run | Min<br>(sec)                         | 95% Confidence Interval |                  |               | Max<br>(sec) |
|-----|--------------------------------------|-------------------------|------------------|---------------|--------------|
|     |                                      | Low<br>(sec)            | Average<br>(sec) | High<br>(sec) |              |
| R   | Timed Out (> 150 hours) 16/16 Trials |                         |                  |               |              |
| G   | 4,424                                | 53,805                  | 71,687           | 89,570        | 224,963      |

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E.g., EverLost

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E.g., Importance of handling imperative as well as declarative specifications?

# Future?

- Absorbing useful ideas from other “styles” generates good results.
- Mix and match!
- E.g., I conjecture a strong underlying connection between abstraction and coverage.



# Conclusion

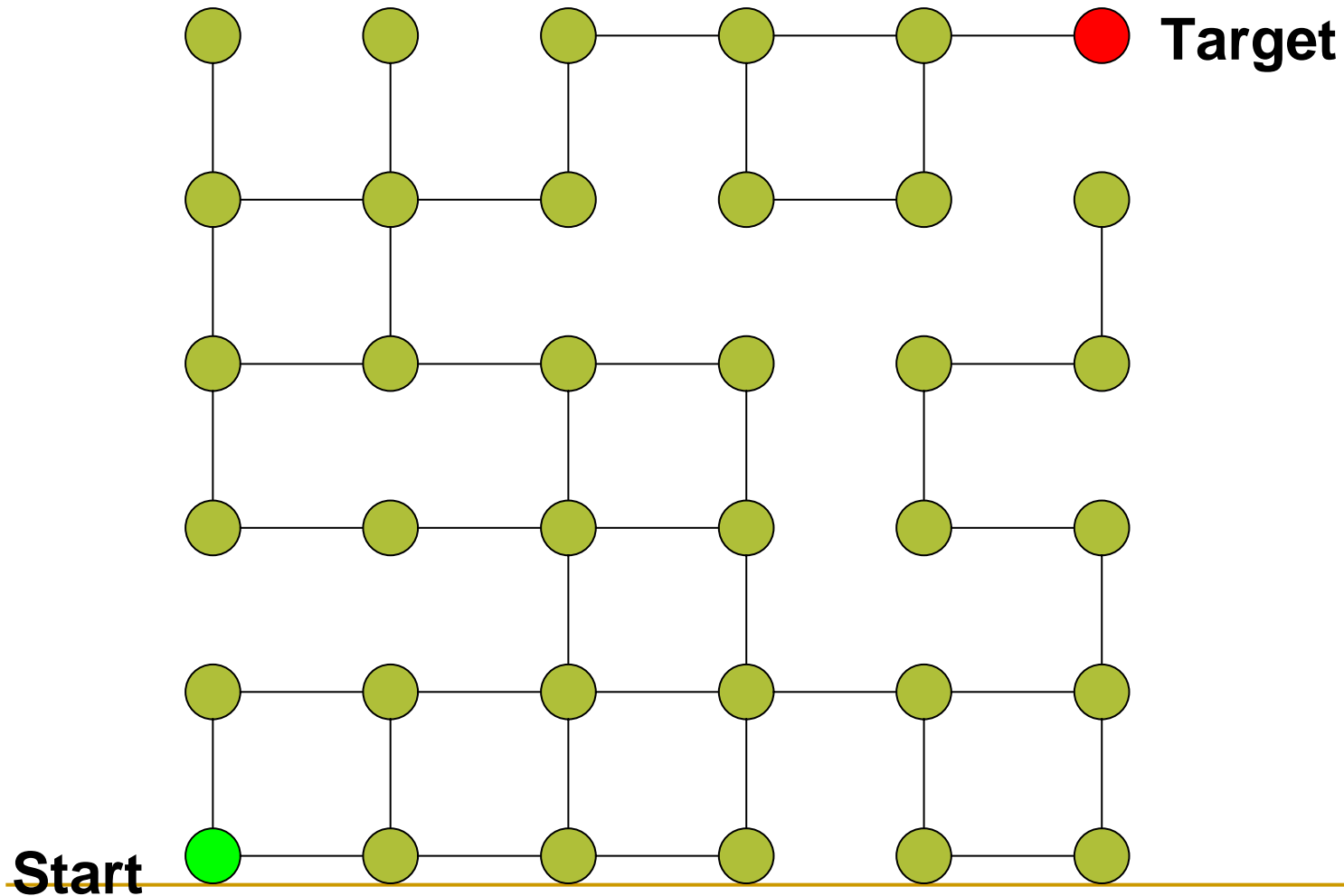
- Train hard in your own style.  
Expertise and depth are your foundation.
- Cross-Train: Friendly sparring with other styles to illuminate your assumptions.
- Learn from other masters, too.
  - This doesn't apply just to verification!
- You can become the Bruce Lee of verification!

# Conclusion

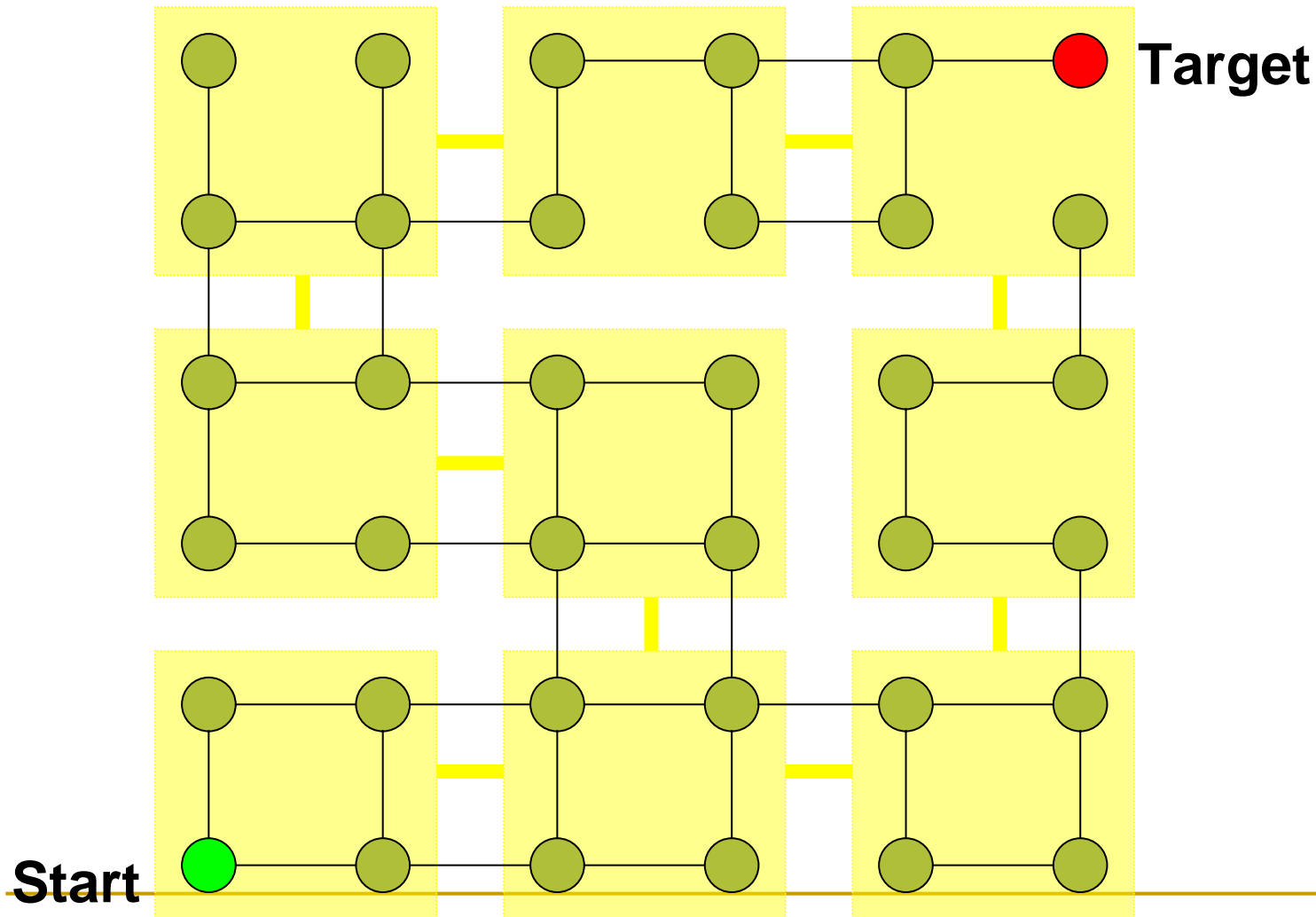
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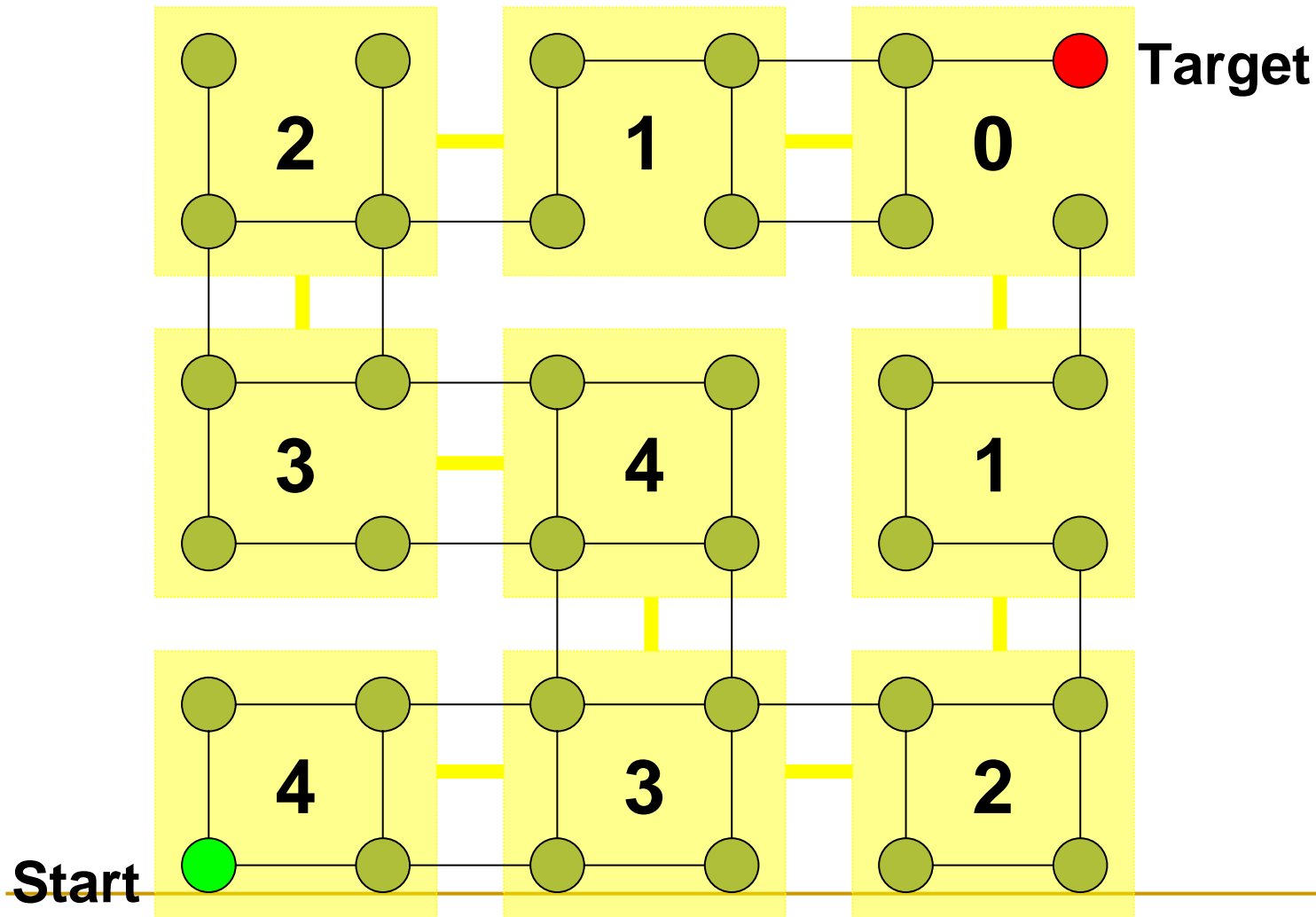
# Simulation is search on concrete state space...



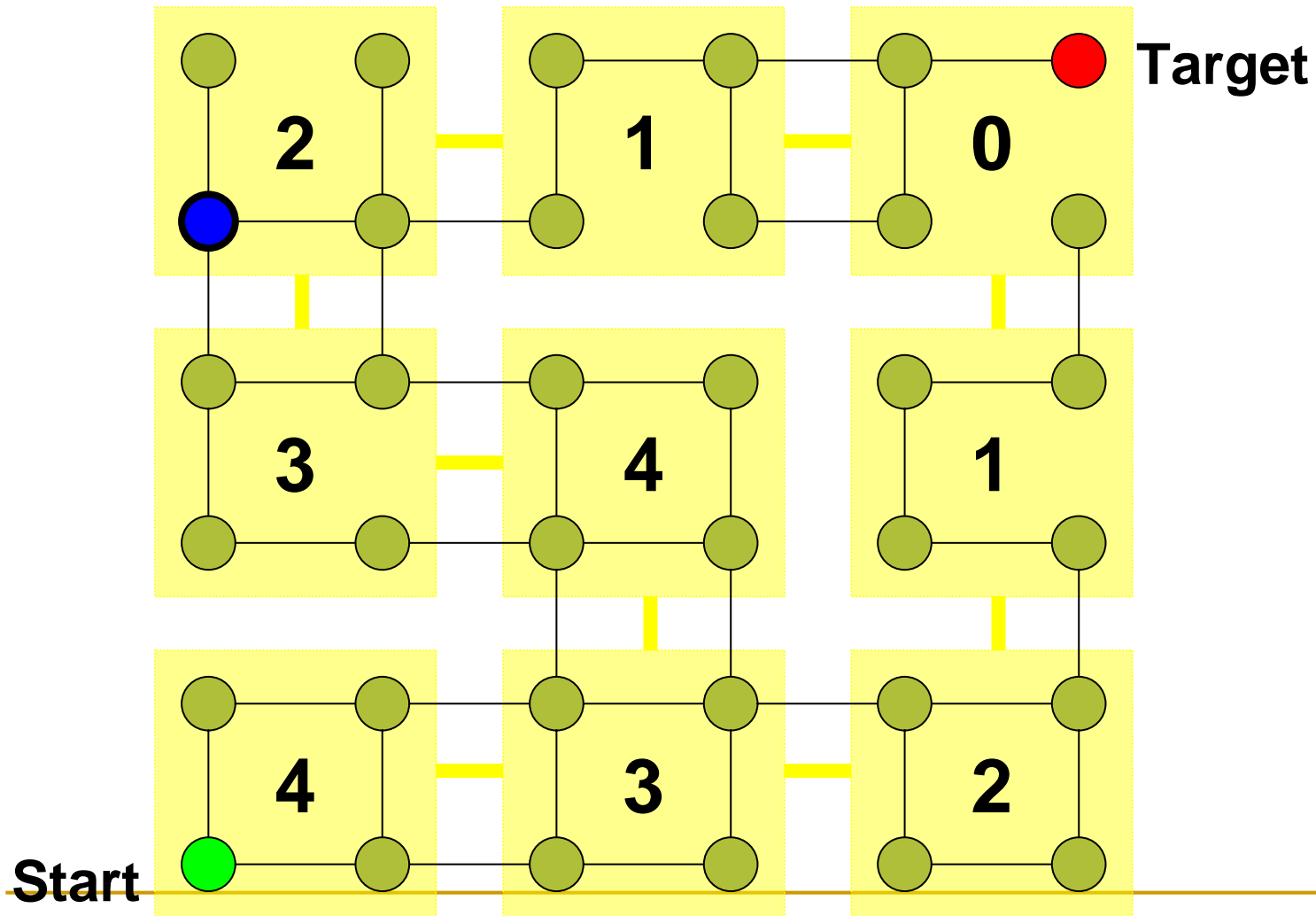
# Abstraction groups states together, reducing state space by losing information...



**Abstract state space can be model checked.**  
**Abstract states can be ranked by abstract distance.**



# Use abstract distances to guide simulation...



# Leaky Abstractions...

