



IBM Haifa Verification Conference – Program

October 23, 2007

<p>9:00 Registration</p> <p>9:15 Opening Remarks Oded Cohn, IBM Haifa Research Lab</p> <hr/> <p>Keynote Talk Session chair: Moshe Levinger</p> <hr/> <p>9:45 Microprocessor Verification Challenges Bob Bentley, Intel Corporation</p> <p>10:45 Break</p> <hr/> <p>Session I: Hardware Verification Session chair: Avi Ziv</p> <hr/> <p>11:15 Invited talk: Out of Steam? - From "Hardware Verification Crisis" to "Crisis of Verification" Wolfgang Roesner, IBM Austin</p> <p>12:00 On the Characterization of Until as a Fixed Point Under Clocked Semantics Dana Fisman</p> <p>12:30 Reactivity in SystemC Transaction-Level Models Frederic Doucet, R.K. Shyamasundar, Ingolf H. Krueger, Saurabh Joshi, and Rajesh K. Gupta</p>	<p>13:00 Lunch</p> <hr/> <p>Session II: Model Checking Session chair: Bob Kurshan</p> <hr/> <p>14:15 Verifying Parameterised Hardware Designs via Counter Automata Ales Smrcka and Tomas Vojnar</p> <p>14:45 How Fast and Fat is your Probabilistic Model Checker? David N. Jansen, Joost-Pieter Katoen, Marcel Oldenkamp, Mariëlle Stoelinga, and Ivan Zapreev</p> <p>15:15 Break</p> <hr/> <p>Session III: Dynamic Hardware Verification Session chair: Bob Bentley</p> <hr/> <p>15:45 Constraint Patterns and Search Procedures for CP-Based Random Test Generation Anna Moss</p> <p>16:15 Using Virtual Coverage to Hit Hard-To-Reach Events Laurent Fournier and Avi Ziv</p> <p>16:45 Cocktail party</p>
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October 24, 2007

<hr/> Session I: HVC Award Session chair: Roderick Bloem <hr/> <p>9:15 Best Paper and HVC Award Presentations</p> <p>9:30 HVC Award Winner: Symbolic Execution and Model Checking for Testing Corina Pasareanu, NASA Ames Research Center</p> <p>10:30 Speed Networking Session</p> <hr/> Session II: Merging Formal and Testing Session chair: Laurent Fournier <hr/> <p>11:15 Invited talk: Simulation vs. Formal: Absorb what is useful; reject what is useless (The Bruce Lee Approach to Verification) Alan Hu, Univ. of British Columbia</p> <p>12:00 Test Case Generation for Ultimately Periodic Paths Saddek Bensalem, Doron Peled, Hongyang Qu, Stavros Tripakis, and Lenore Zuck</p> <p>12:30 Dynamic Testing via Automata Learning Harald Raffelt, Bernhard Steffen, and Tiziana Margaria</p>	<p>13:00 Lunch</p> <hr/> Session III: Large Systems Verification Session chair: Alan Hu <hr/> <p>14:15 Invited talk: Scaling Commercial Verification to Larger Systems Robert Kurshan, Cadence</p> <p>15:30 Excursion</p>
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October 25, 2007

Keynote Talk Session chair: Sharon Barner 9:30 From Hardware Verification to Software Verification: Re-use and Re-learn Aarti Gupta, NEC Labs America 10:30 Break	Software Bugs Session chair: Eitan Farchi 14:15 Invited talk: Where Do Bugs Come From? Andreas Zeller, Saarland University 15:15 Locating Regression Bugs Dor Nir, Shmuel Tyszberowicz, and Amiram Yehudai, 15:45 Break
Formal Verification for Software Session chair: Aarti Gupta 11:00 On the Architecture of System Verification Environments Mark A. Hillebrand and Wolfgang J. Paul 11:30 Exploiting Shared Structure in Software Verification Conditions Domagoj Babic and Alan J. Hu 12:00 Delayed Nondeterminism in Model Checking Embedded Systems Assembly Code Thomas Noll and Bastian Schlich 12:30 A Complete Bounded Model Checking Algorithm for Pushdown Systems Gerard Basler, Daniel Kroening, and Georg Weissenbacher 13:00 Lunch	Software Testing Session chair: Shmuel Ur 16:15 The Advantages of Post-link Code Coverage Orna Raz, Moshe Klausner, Nitzan Peleg, Gad Haber, Eitan Farchi, Shachar Fienblit, Yakov Filiarsky, Shay Gammer, and Sergey Novikov 16:45 GenUTest: A Unit Test and Mock Aspect Generation Tool Benny Pasternak, Shmuel Tyszberowicz, and Amiram Yehudai 17:15 Closing Remarks