Path Based System Level Stimuli Generation

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Simulation-Based Verification Methods
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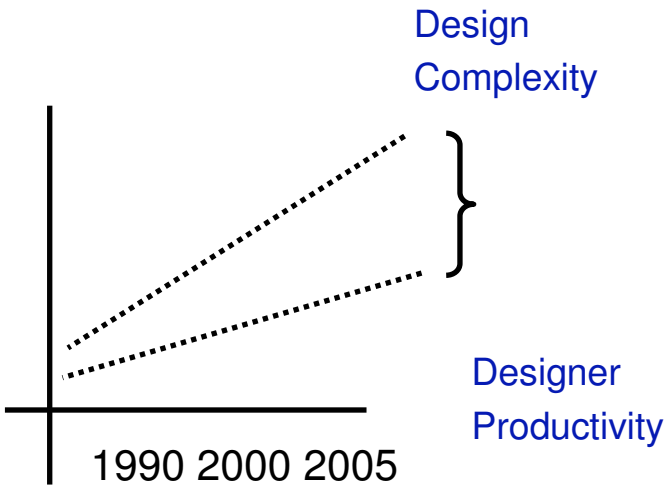
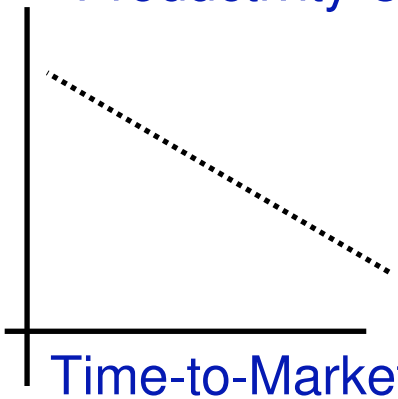
Background

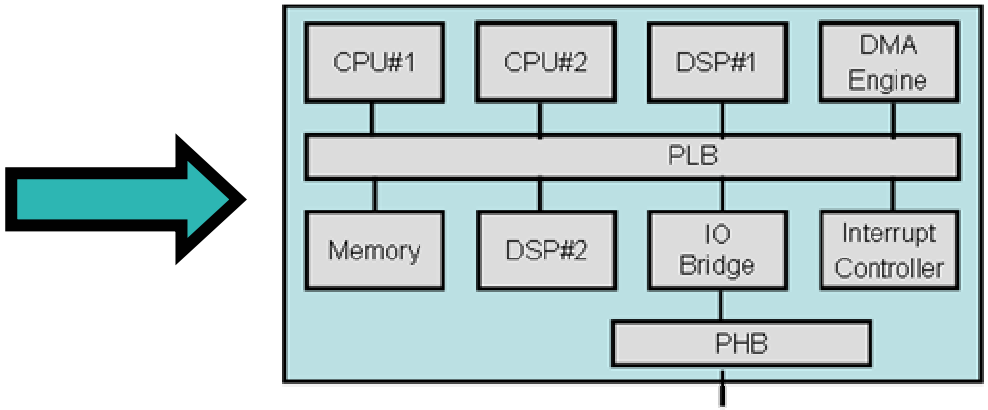


Productivity Gap



Time-to-Market Trend

System-on-a-Chip (SoC) Methodology

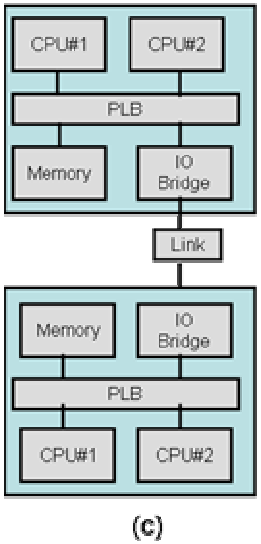


System Verification

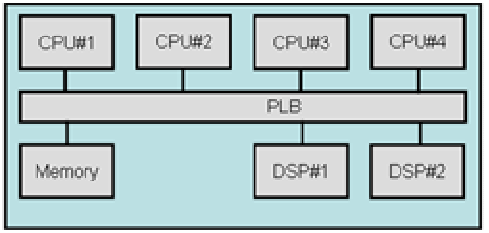
System verification is aimed at validating the integration of several previously verified cores in a relatively short time.

Challenges in System Level Stimuli Generation

- Specifying system level scenarios in an abstract form
  - While generating required low level stimuli
- Generating coordinated stimuli between cores
- Reusing of test specification and verification environment code
- Quickly adapting to configuration topology changes
- Adapting to new cores



(c)



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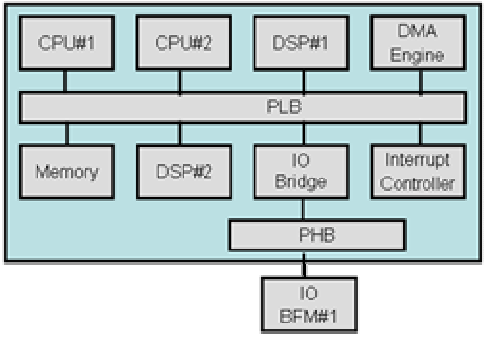
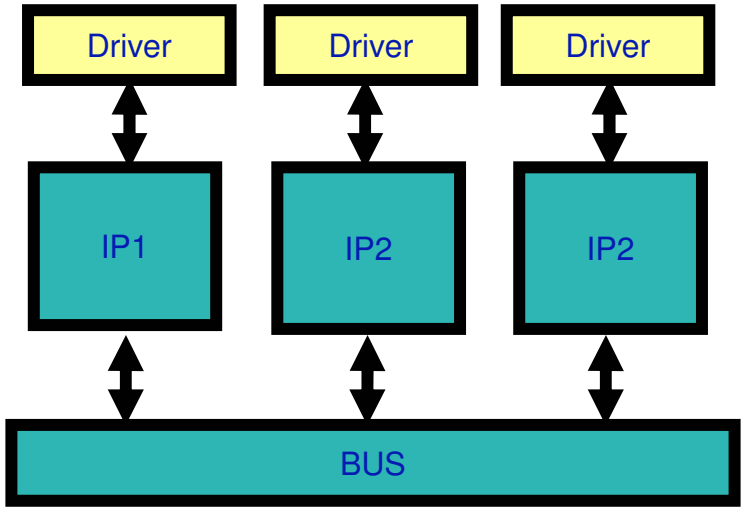


(b)

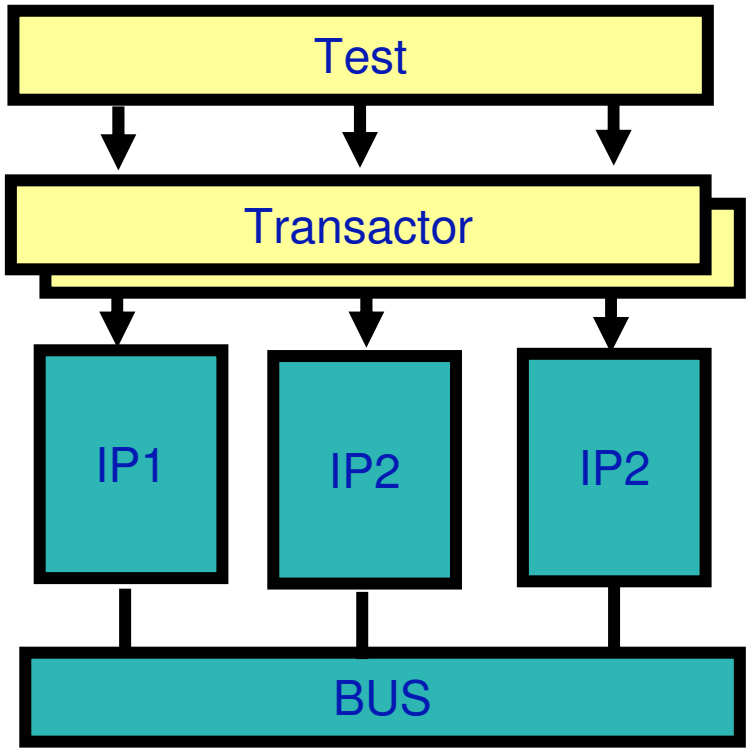
Approach #1: Combining Lower Level Drivers

- Advantages
  - Simple
  - Quickly adapts to new cores
  - Reuse of core VIP
- Disadvantages
  - Not system level verification
    - No coordinated stimuli
    - No system level scenarios



Approach #2: Transaction Based Verification

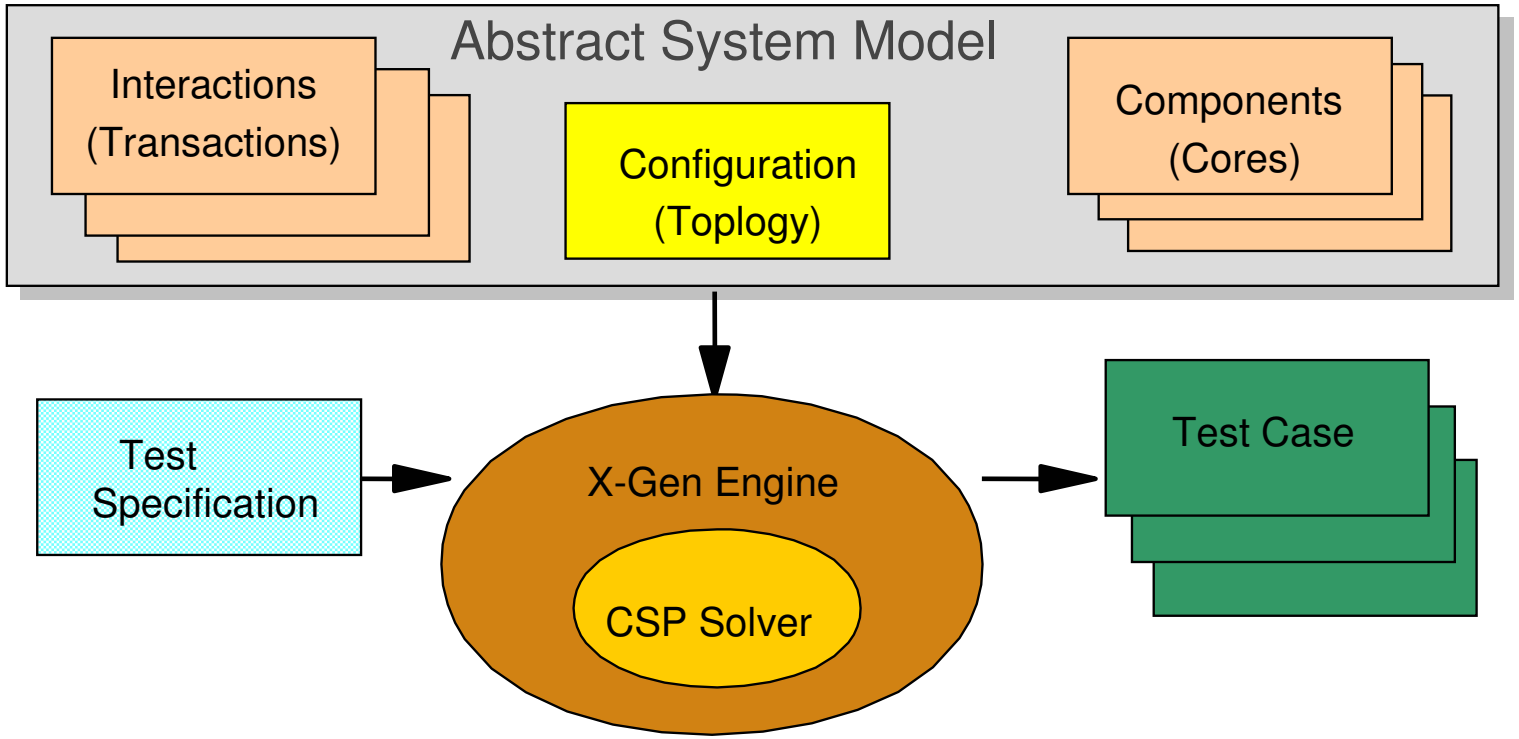
- Advantages
  - System level abstraction
  - Allows complex coordinated stimuli
  - Allows reuse of test specification
- Disadvantages
  - Transactor code is monolithic
  - Difficult to adapt to configuration changes
  - Difficult to adapt to new components / changed functionality



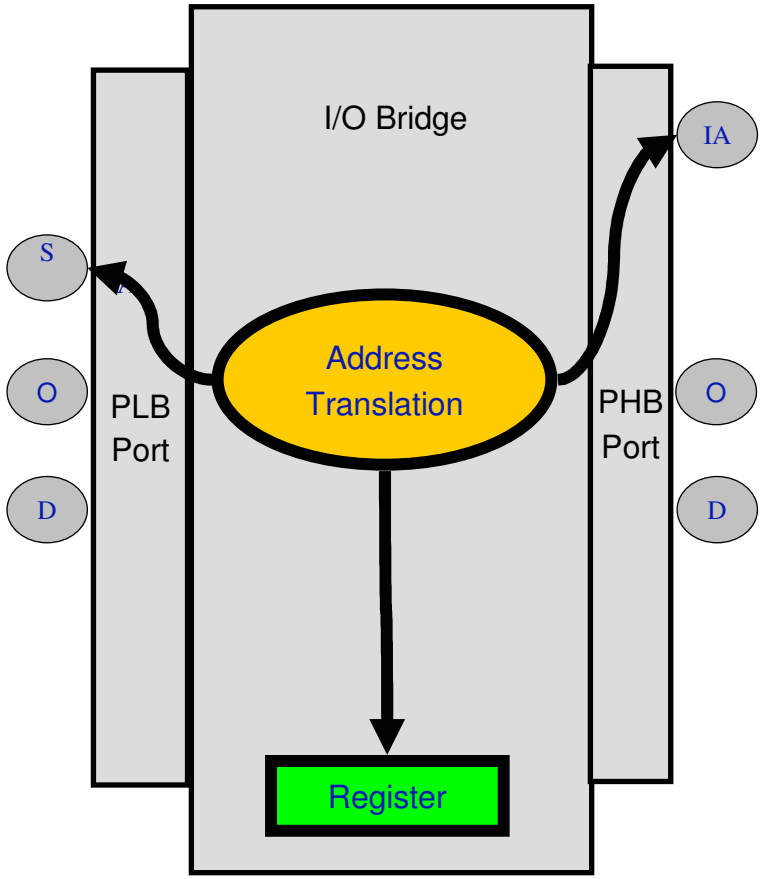
X-Gen

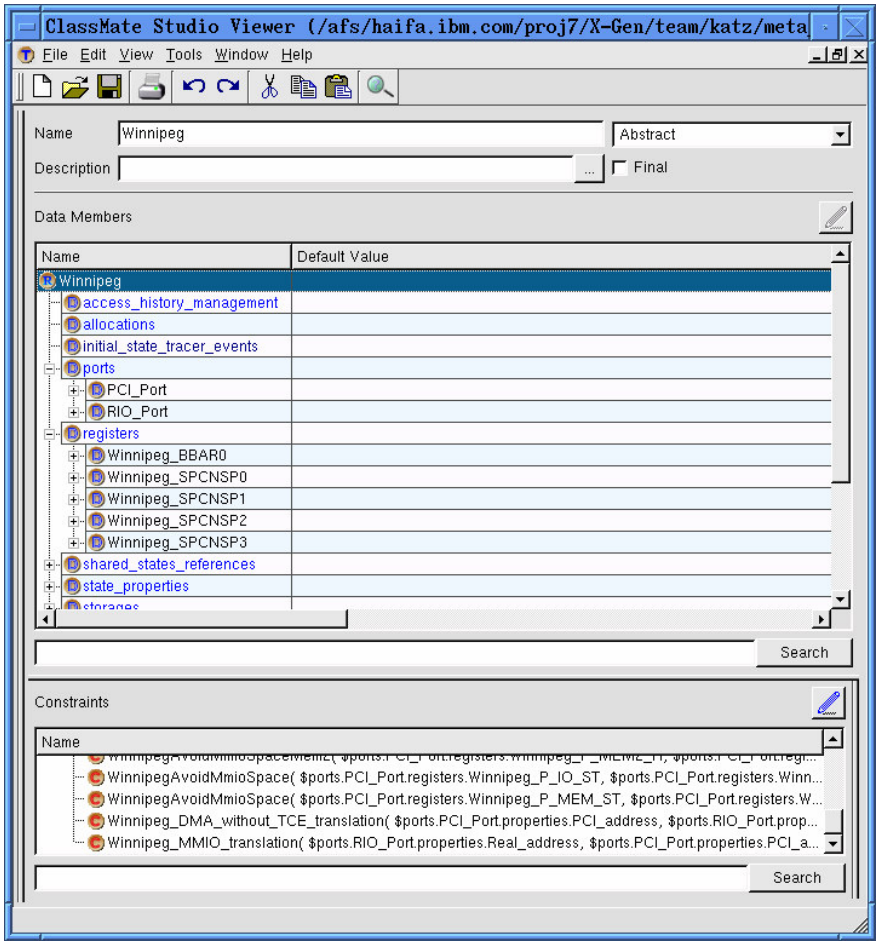
- IBM's state-of-the-art system-level stimuli generator
- Focus on the system as a whole, including
  - Processors
  - Memory sub-system
  - Complex interconnect (bridges, clustering)
  - I/O

X-Gen Overview



Component (Core) Behavior



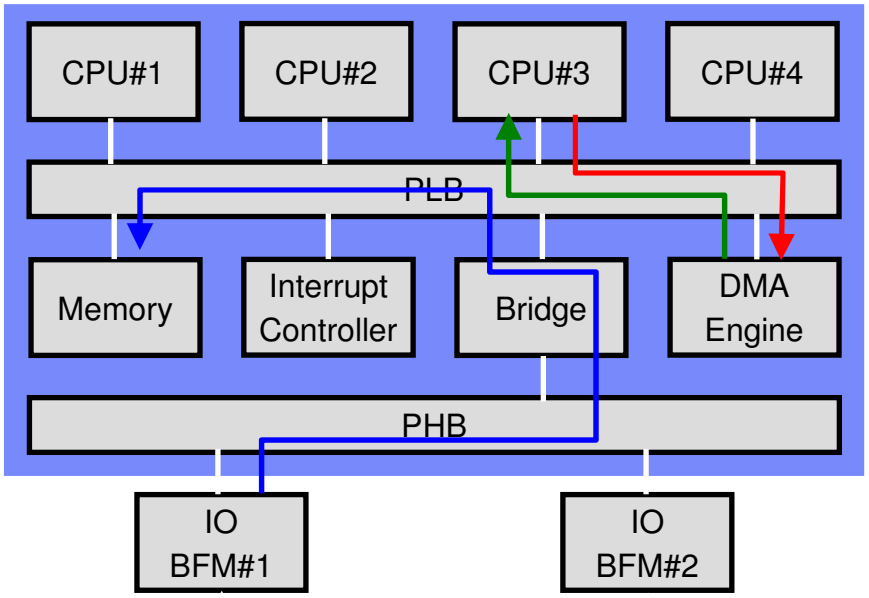


Interactions (Transactions)

- **Interaction**: Acts, Actors

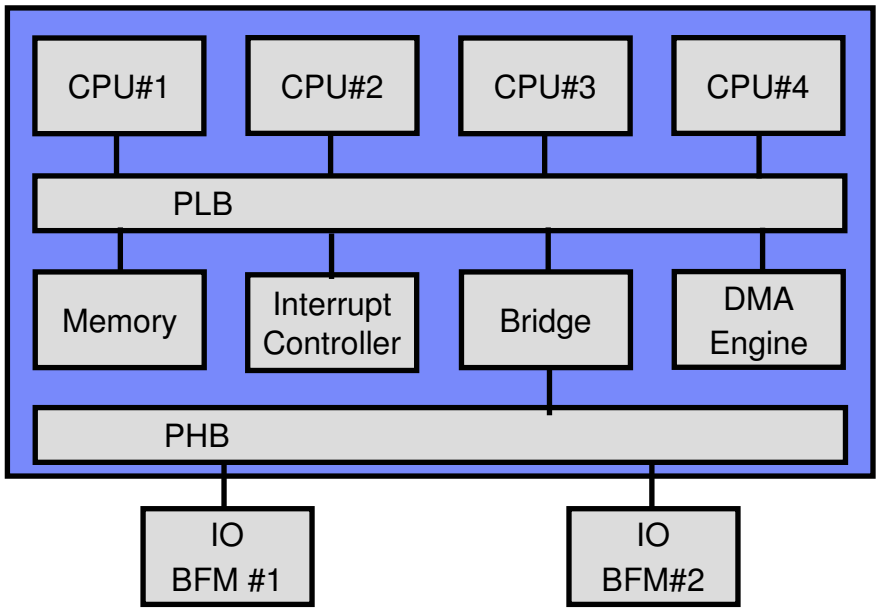
A DMA Interaction

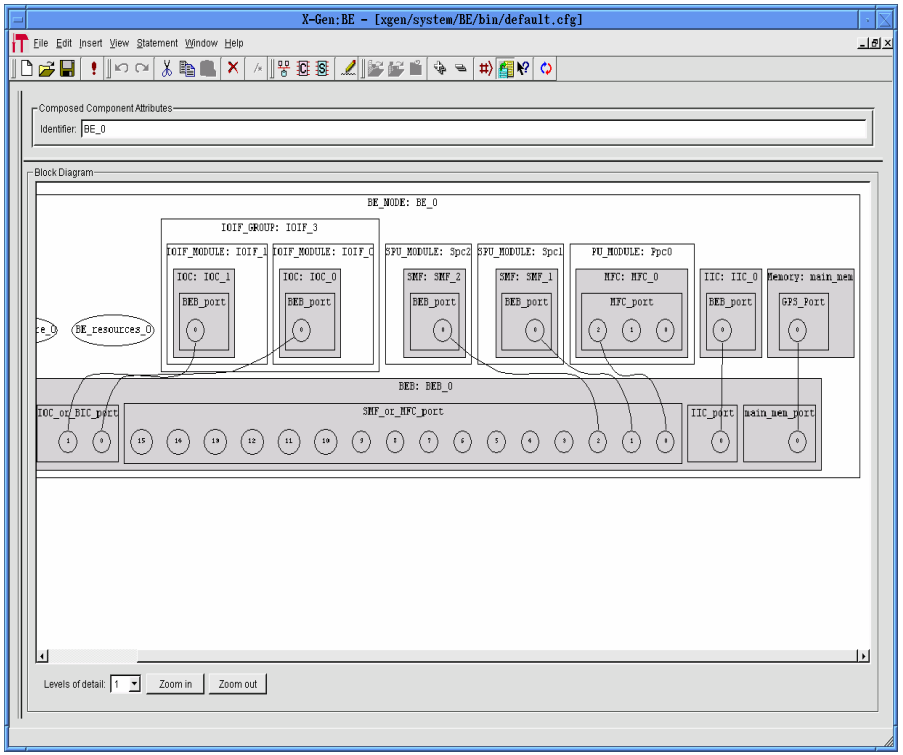
- A CPU stores to the doorbell register of the DMA engine
- The data is moved from the IO port to memory
- The DMA engine interrupts the initiating CPU



Configuration

- Represents the physical and logical connection between components



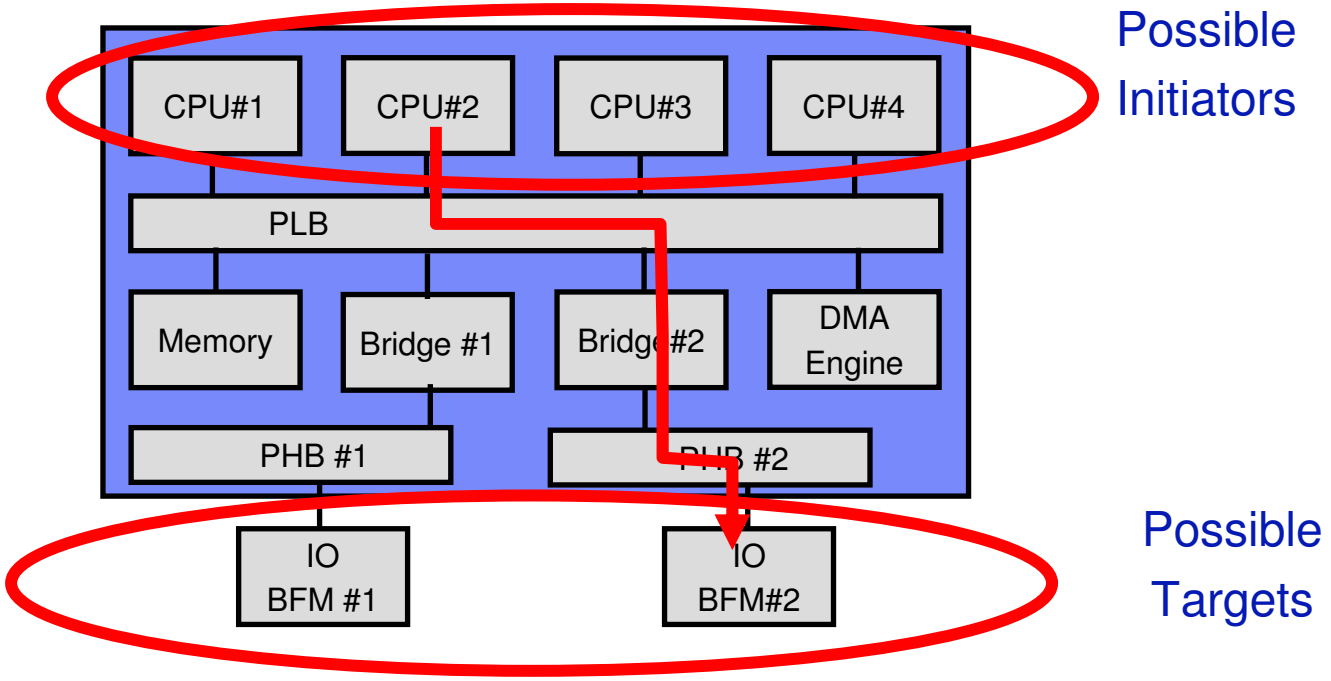


X-Gen Generation Scheme

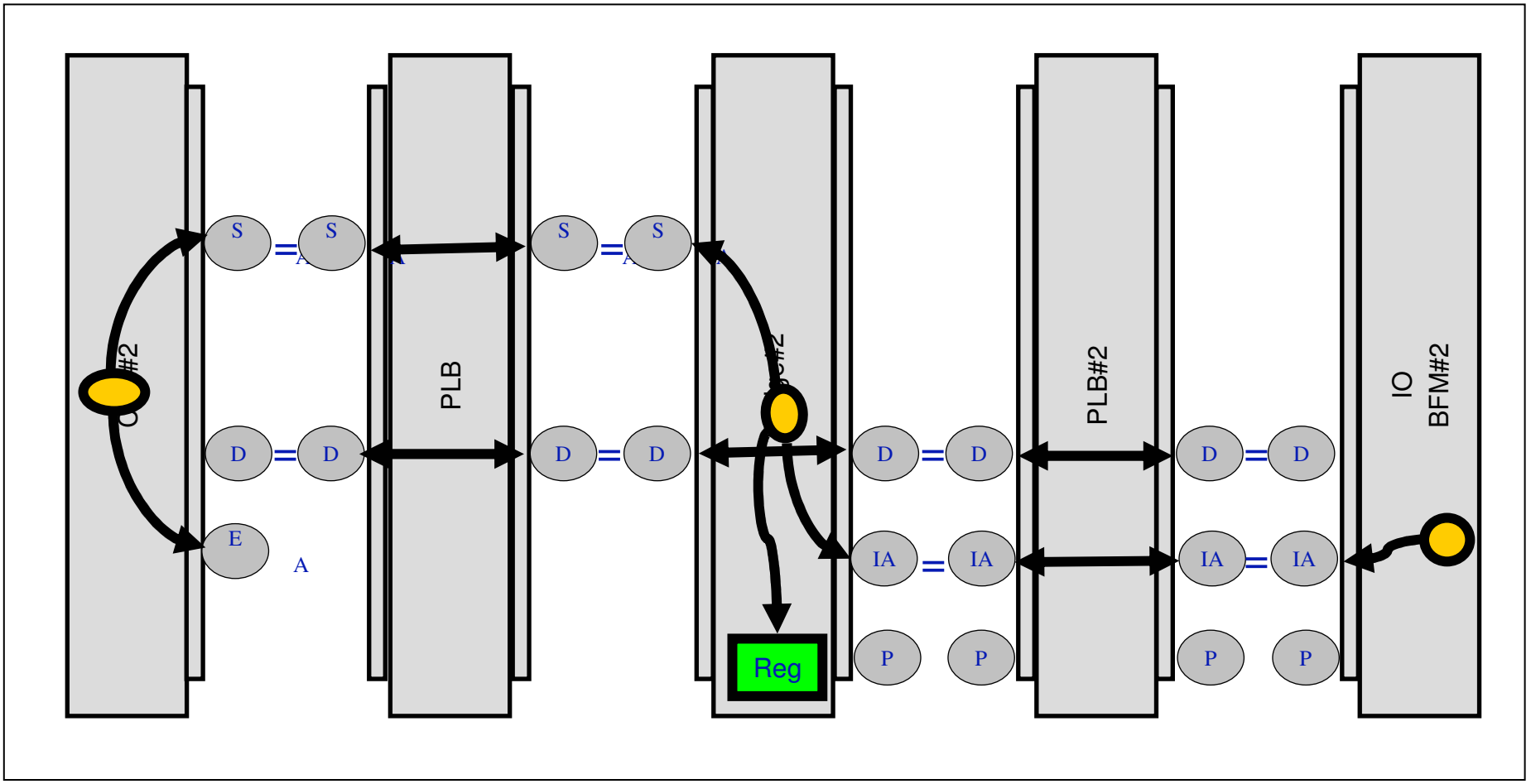
- For each interaction in the test specification
  1. Select the participating components and the path(s) between them
  2. Select the values of relevant properties of the participating components (e.g. io_address, system_address, data)
  3. Initialize the relevant test case resources (data memory, translation tables, processor instructions, BFM commands)

X-Gen Generation Scheme – Path selection

- Example interaction: CPU_to_BFM_MMIO



X-Gen Generation Scheme – Property Selection



Advantages

- Adapts well to configuration changes

DUT change	Pure transaction modelling change	X-Gen changes
New component of existing type	Modify multiple transactors	Change configuration
Changes to existing component	Modify multiple transactors	Modify component
New component with same interactions	Modify multiple transactors	New component
New system level interaction	New transactor	New interaction + Modify components

More Advantages

- Coordinated stimuli between interactions
  - Generation state is maintained in the components
- Scalable CSP solution
  - Can handle dozens of components and thousands of possible paths
- Disadvantages
  - Modeling requires expertise
  - CSP partitioning limitations

X-Gen's Track Record

- Used in IBM's state of the art systems verification
  - Low to high end PowerPC servers
    - Dozens of processors
    - IO interfaces (e.g. PCIX/E, HyperTransport)
    - Complex clustering architectures (e.g. Infiniband)
  - Gaming Technologies
    - PowerPC and propriety processors
    - Dedicated DMA engines
- Assisted in discovery of hundreds of hardware bugs