IBM Haifa Leadership Seminar - Agenda

IBM Verification Seminar 2004

November 21, 2004

9:15 Arrival

9:30 Welcome,
David Bernstein, Mgr., Software and Verification Technologies, IBM Haifa Labs

9:45 *Formal Verification of Synchronizers in GALS SoCs*,
Ran Ginosar, Head, VLSI Systems Research Center, Electrical Engineering Department, Technion - Israel Institute of Technology

10:25 *A Massively Parallel Platform for Formal Verification: RuleBase Parallel Edition*,
Rachel Tzoref, IBM Haifa Labs

10:55 *SystemVerilog: Introduction and a User Perspective*,
Johny Srouji, Engineering Manager, Intel CAD Division, Haifa

11:25 Coffee break

11:40 *State of the Technology Industry in Israel... and the Future*,
Orna Berry, Venture Partner in Gemini Israel Funds and Former Chief Scientist of the Israeli Ministry of Industry and Trade

12:20 *EDA Standards: Motivation, Players, Challenges, and Achievements*,
Dennis Brophy, Chair, Accellera Standards Organization and Director of Strategic Business Development, Model Technology

12:50 *Piparazzi: A Micro-architecture Approach to Functional & Performance Verification in Processors*,
Eyal Bin, IBM Haifa Labs

13:20 Lunch

14:30 Keynote: *Predicate Abstraction and Refinement Techniques for Verifying Verilog*,
Ed Clarke, FORE Systems Professor of Computer Science and Professor of Electrical and Computer Engineering, Carnegie Mellon University

15:30 Break

15:45 *Debugging complex FPGA platforms*,
Ivo Bolsens, Vice President and Chief Technology Officer, Xilinx

16:15 *Panel: HVL vs. HDVL*,
Panelists: Coby Chanoch, Verisity; Jay Lawrence, Cadence Design Systems; Kobi Pines, Marvell Technology Group; Rob Slater, FreeScale Semiconductor,

17:00 Concluding Remarks,
Michael Rodeh, Director, IBM Haifa Labs