# IBM Haifa Conference – Agenda

## 3rd HiPEAC Industrial Workshop on Compilers and Architectures

**Organized by IBM Research Lab in Haifa, Israel**

**April 17, 2007**

www.haifa.il.ibm.com/Workshops/compiler2007/

**09:30** Welcome
*Oded Cohn, HRL*

### Session 1
### Making Better Use of Hardware

**09:45** Initial Results of the Performance Implications of Thread Migration on a Chip Multi-Core
*Y. Sazeides, L. He, C. Ioannou, P. Charalambous, University of Cyprus, Nicosia, Cyprus, P. Michaud, D. Fetis, A. Seznec, Irisa-Inria, Rennes, France*

**10:15** Caravela: A Distributed Stream-based Computing Platform
*Leonel Sousa, Shinichi Yamagiwa, INESC-ID/IST, TULisbon*

**10:45** Probabilistic Cache Filtering
*Yoav Etsion, Dror G. Feitelson, Hebrew University, Jerusalem*

**11:15** Coffee break

### Session 2
### Compiler Optimizations

**11:35** Data Layout Optimizations in GCC
*Olga Golovanevsky, Razya Ladelsky, IBM HRL*

**12:05** SIMDinator: Use of the x86 SIMD Instructions
*David Livshin, DALsoft*

**12:35** Issues and Challenges in Compiling for Multiple Forms of Parallelism, in IBM Research Compilers
*Kathryn O'Brien, IBM T.J. Watson Research Center*

**13:05** Lunch and informal discussions

**14:10** **Keynote: A Highly Programmable C/GPU**
*Peter Hofstee, IBM Distinguished Engineer, Chief Architect of the Cell Synergistic Processor, Cell Chief Scientist*

**15:00** Implementation and Validation of a Cell Simulator using UNISIM
*Felipe Cabarcas, Alejandro Rico, David Rodenas, Xavier Martorell, Alex Ramirez, Eduard Ayguade, UPC*

**15:30** Coffee break

### Session 3
### Making Better Use of Parallelism

**15:50** CAPSULE: Parallel Execution of Component-based Programs
*Pierre Palatin, Zheng Li, Yves Lhuillier, Olivier Temam, INRIA*

**16:20** Using Extremely Fine Granularity Multithreading for Energy Efficient Computing
*Alex Gontmakher, Avi Mendelson, Assaf Schuster, Technion*

**16:50** How Many Cores is Too Many Cores?
*Avi Mendelson, Intel*

**17:20** Concluding remarks
*David Bernstein, HRL*